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(54) Method for evaluating epitaxial layers and test pattern for process evaluation.

(57) In a method for evaluating thickness of a semiconductor layer (20) epitaxially growing on a main surface of a substrate (1), a plurality of stripe-shaped ridges (12) extending in a prescribed direction are formed on the surface of the substrate, and a semiconductor layer (20) is epitaxially grown on the surface of the substrate including the stripe-shaped ridges while irradiating the stripe-shaped ridges with light (21) and monitoring diffracted light (22,23) from the stripe-shaped ridges to evaluate the thickness of the epitaxially growing semiconductor layer. Therefore, the thickness of the epitaxial layer is evaluated with high precision during the epitaxial growth process.

Fig.3 (a)

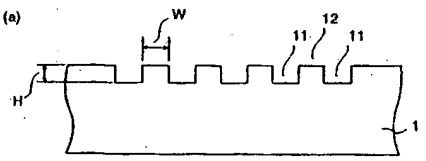


Fig.3 (b)

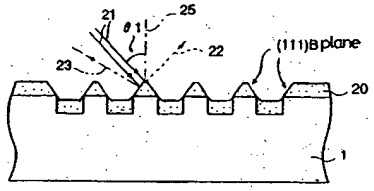
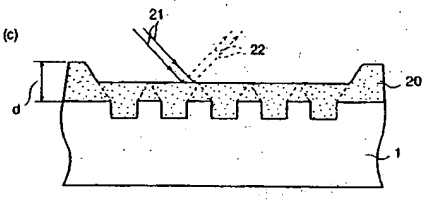


Fig.3 (c)



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FIELD OF THE INVENTION

The present invention relates to a method for evaluating a semiconductor layer epitaxially grown on a substrate and, more particularly, to a method for evaluating the thickness of that layer during the epitaxial growth process with high precision.

The present invention also relates to a test pattern for process evaluation which is disposed on a substrate and used for evaluating semiconductor layers epitaxially grown on the substrate.

The present invention also relates to a method for evaluating an AlGaAs multiple quantum well layer and, more particularly to a method for evaluating the thickness and Al composition of the multiple quantum well layer with high precision.

BACKGROUND OF THE INVENTION

Figures 17(a) and 17(b) are perspective views for explaining a conventional method for measuring the thickness of a semiconductor layer epitaxially grown on a substrate. In these figures, reference numeral 101 designates a GaAs substrate and numeral 102 designates an epitaxial layer grown on the GaAs substrate 101.

Initially, as illustrated in figure 17(a), an epitaxial layer 102 is grown on the GaAs substrate 101 having a diameter of 2 inches by MOCVD. The thickness of the epitaxial layer 102 is controlled by the growth time according to the growth rate obtained by the quantity of the supplied source gas. Thereafter, this wafer is cleaved to make a strip sample 103 shown in figure 17(b), and the section of the sample 103 is observed with a scanning electron microscopy (SEM) and photographed, whereby the thickness of the epitaxial layer is obtained.

In the conventional evaluation method, however, the cleaving of the wafer takes much time and labor. In addition, since the evaluation is performed after the growth of the epitaxial layer, a feedback cannot be applied during the epitaxial growth, so that the controllability of the thickness is poor, resulting in a poor production yield.

Figure 18 is a schematic diagram illustrating a crystal growth monitor apparatus for optically measuring thickness of an epitaxial layer grown on a semiconductor substrate by molecular beam epitaxy (MBE). This apparatus is disclosed in, for example, Japanese Published Patent Application No. Hei. 2-252694.

In figure 18, a ultra-high vacuum container 111 having an observation window 112 contains a substrate holder 113 on which a substrate 114 is disposed. In the ultra-high vacuum container 111, molecular or atomic beam of materials, which is produced by evaporating material sources 115 and 116, reaches the substrate 114, whereby a crystal is grown on the substrate. Reference numeral 117 designates a light source, numeral 119 designates a half mirror for separating reflected light from the substrate 114, numeral 120 designates a condenser lens, numeral 121 designates a diaphragm, and numeral 123 designates an eyepiece. Light 118 emitted from the light source 117 travels through the half mirror 119, the condenser lens 120, the diaphragm 121, and the observation window 112 and reaches the surface of the crystal layer growing on the substrate. The light is reflected at the surface of the growing crystal layer and received by the half mirror 122. The half mirror 122 is observed with the eyepiece 123 to see if the light strikes the proper position on the surface of the substrate. The optical path is adjusted if necessary. On the other hand, the light reflected at the surface of the growing crystal layer is reflected by the half mirror 119. The reflected light 124 is received by a spectroscope 125 and turned into monochromatic light. This monochromatic light is guided through a condenser lens 126 to a Rochon prism 127. In the Rochon prism 127, the monochromatic light is divided into two beams having different polarization planes that are at right angles to each other. These two light beams are respectively received by PIN photodiodes 128 and 129 having similar characteristics. These photodiodes 128 and 129 are connected in series and in reversed polarity, and the difference output is amplified by a DC amplifier 130 and recorded in a recorder 131.

A polarized light caused by reflection at the surface of the growing crystal layer varies according to the crystal growth condition. For example, in a GaAs growth, a polarized light attains the maximum when an atomic plane of Ga (As) is formed. Thereafter, the polarized light gradually decreases as As (Ga) molecules are accumulated on the atomic plane and, finally, becomes the minimum. When an As (Ga) atomic plane is again formed, the polarized light becomes the maximum again. Therefore, if orthogonal polarization components are taken out and a difference between them is measured, the growth process at the surface of the substrate is directly observed.

Figure 19 illustrates the result of observation of a growing GaAs crystal using the crystal growth monitor apparatus shown in figure 18, in which the abscissa shows the growth time and the ordinate shows the output from the DC amplifier 130. This output corresponds to a difference in intensities of the orthogonal polarization components. In addition, the output from the DC amplifier 130 shows a damped oscillation, and a period of this damped oscillation corresponds to the growth of one atomic layer. Therefore, the thickness of the growing crystal layer can be obtained by counting the periods.

In the prior art crystal growth monitor apparatus, however, since the thickness of the growing crystal layer is measured by detecting the variation in the reflected light due to the atomic layer level unevenness at the surface of the crystal layer, the variation in the output signal is very small, resulting in a difficulty in the measurement. In addition, in order to increase the S/N ratio, means for polarizing the incident light is required, whereby the monitor apparatus is complicated and rises in price.

Figures 20(a) and 20(b) are perspective views for explaining a prior art method for evaluating an AlGaAs multiple quantum well (hereinafter referred to as MQW) layer. In these figures, reference numeral 201 designates a GaAs substrate. A first $Al_{0.4}Ga_{0.6}As$ layer 202 is disposed on the GaAs substrate 201. An MQW layer 203 comprising alternating $Al_{0.1}Ga_{0.9}As$ well layers and $Al_{0.3}Ga_{0.7}As$ barrier layers is disposed on the first $Al_{0.4}Ga_{0.6}As$ layer 202. A second $Al_{0.4}Ga_{0.6}As$ layer 204 is disposed on the MQW layer 203.

A description is given of the evaluation process.

Initially, as illustrated in figure 20(a), there are successively grown on the 2-inch diameter GaAs substrate 201 the first $Al_{0.4}Ga_{0.6}As$ layer 202, the MQW layer 203 comprising alternating $Al_{0.1}Ga_{0.9}As$ well layers and $Al_{0.3}Ga_{0.7}As$ barrier layers, and the second $Al_{0.4}Ga_{0.6}As$ layer 204, preferably by MOCVD. The thicknesses of these layers are controlled by the growth time according to the growth rate obtained by the quantity of the supplied source gas. Thereafter, as illustrated in figure 20-(b), the wafer is cleaved to make a strip sample 205, and the section of the sample 205 is observed with an SEM and photographed, whereby the thicknesses of the respective layers are evaluated. Further, the Al compositions of the respective layers are evaluated by peak wavelengths obtained in a PL (photoluminescence) evaluation at room temperature.

In the above-described evaluation process of the thickness of the AlGaAs MQW layer, however, the cleaving of the wafer takes much time and labor. In addition, a precision enough to detect an error of several nanometer cannot be achieved. In the evaluation of the Al composition, the PL peak wavelength varies due to variations in the thickness and the Al composition, and the variation in the Al composition cannot be separated from the variation in the thickness. Therefore, an accurate evaluation of the Al composition is impossible.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a relatively simple method for evaluating epitaxial layers during the epitaxial growth process.

It is another object of the present invention to provide a test pattern for process evaluation that realizes a precise evaluation of epitaxial layers grown on a substrate.

It is still another object of the present invention to provide a method for evaluating thickness and Al composition of an AlGaAs MQW layer with high precision, without cleaving a wafer.

Other objects and advantages of the present invention will become apparent from the detailed description give hereinafter; it should be understood, however, that the detailed description and specific embodiment are given by way of illustration only, since various changes and modifications within the scope of the invention will become apparent to those skilled in the art from this detailed description.

According to a first aspect of the present invention, in a method for evaluating a semiconductor layer epitaxially growing on a substrate, a plurality of stripe-shaped ridges extending in a prescribed direction are formed on the substrate, and a semiconductor layer is grown on the substrate including the stripe-shaped ridges while irradiating the stripe-shaped ridges with light and monitoring diffracted light from the stripe-shaped ridges, whereby the thickness of the epitaxially grown semiconductor layer is evaluated. Therefore, the thickness of the epitaxial layer is easily evaluated during the epitaxial growth process, whereby the thickness controllability is significantly improved.

According to a second aspect of the present invention, a test pattern comprises a plurality of stripe-shaped ridges formed on a part of a substrate and in a prescribed direction selected so that a semiconductor layer having a triangle section and side surfaces on which the epitaxial growth does not proceed is grown on each of the stripe-shaped ridges. Each ridge has a width W and a height H that satisfy a relation of $d \fallingdotseq 0.7W + H$ where d is a desired thickness of the semiconductor layer epitaxially grown on the substrate. Since the test pattern comprising the stripe-shaped ridges are flatly embedded when the epitaxially growing layer reaches the desired thickness, the thickness of the epitaxially growing layer is evaluated with high precision.

According to a third aspect of the present invention, in a method for evaluating an epitaxially grown AlGaAs multiple quantum well layer, initially, an insulating mask pattern having an opening is formed on a part of a substrate on which a plurality of semiconductor layers including the AlGaAs multiple quantum well layer are to be grown. The ratio of the width of the opening to the width of the insulating mask pattern is varied continuously or in steps. Then, a plurality of semiconductor layers including the AlGaAs multiple quantum well layer

are grown on the substrate including the insulating mask pattern using a vapor phase growth method. Thereafter, PL peak wavelengths of the AlGaAs multiple quantum well layer grown in the opening of the insulating mask pattern are measured at different positions with different opening ratios of the insulating mask pattern, and the measured values are compared with theoretical curves obtained with respect to a standard quantum well structure, whereby the thickness and the Al composition of the AlGaAs multiple quantum well layer are evaluated. The PL peak wavelengths vary in response to variations in the thickness and the Al composition, and the variation in the PL peak wavelengths at the different positions of the opening of the insulating mask pattern due to the variation in the thickness is different from that due to the variation in the Al composition ratio, so that the thickness and the Al composition ratio of the AlGaAs multiple quantum well layer are evaluated with high precision, without cleaving the wafer.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a plan view of a substrate including a test pattern for process evaluation used for evaluating an epitaxial layer growing on the substrate, in accordance with a first embodiment of the present invention.

Figure 2 is a sectional view taken along a line 2-2 of figure 1.

Figures 3(a)-3(c) are sectional views for explaining the evaluation method according to the first embodiment of the present invention.

Figures 4(a)-4(c) and 5(a)-5(b) are sectional views for explaining reflections of incident light on the surface of the test pattern at different steps in the epitaxial growth process, in accordance with the first embodiment of the present invention.

Figure 6 is a graph illustrating growth time vs. diffracted light intensity characteristics.

Figure 7 is a schematic diagram illustrating an epitaxial growth apparatus employed for the epitaxial layer evaluation method according to the first embodiment of the present invention.

Figure 8 is a perspective view, partially in section, illustrating an InP semiconductor laser including a diffraction grating.

Figures 9(a)-9(c) are sectional views for explaining a method for evaluating an epitaxial layer in accordance with a second embodiment of the present invention, which is employed in the production of the semiconductor laser shown in figure 8.

Figures 10(a)-10(c) are sectional views for explaining a method for evaluating epitaxial layers in accordance with a third embodiment of the present invention.

Figure 11 is a perspective view illustrating a substrate including a test pattern for process evaluation used for evaluating epitaxial layers growing on the substrate, in accordance with a fourth embodiment of the present invention.

Figure 12 is an enlarged view of the test pattern shown in figure 11.

Figure 13 is a graph illustrating insulating mask opening ratio vs. growth rate characteristics.

Figure 14 is a sectional view taken along a line 14-14 of figure 12, illustrating epitaxial layers grown on the substrate exposed in the opening of the insulating mask.

Figure 15 is a graph illustrating well layer thickness vs. PL wavelength characteristics, for explaining the evaluation method according to the fourth embodiment of the present invention.

Figure 16 is a plan view illustrating a variation of the test pattern employed in the evaluation method according to the fourth embodiment of the present invention.

Figures 17(a) and 17(b) are perspective views for explaining a method for evaluating the thickness of a epitaxial layer grown on a semiconductor substrate, according to the prior art.

Figure 18 is a schematic diagram illustrating a crystal growth monitor apparatus for optically measuring the thickness of an epitaxial layer grown on a semiconductor substrate by MBE, according to the prior art.

Figure 19 is a diagram illustrating the result of observation of a growing GaAs crystal using the crystal growth monitor apparatus shown in figure 18.

Figures 20(a) and 20(b) are perspective views for explaining a method for evaluating an AlGaAs MQW layer according to the prior art.

Figures 21(a) and 21(b) are a plan view and a sectional view illustrating a modification of the first embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 is a plan view of a substrate including a test pattern used for evaluating an epitaxial layer grown on the substrate, in accordance with a first embodiment of the present invention. In figure 1, reference numeral 1 designates a GaAs substrate with a (100) surface orientation. The GaAs substrate 1 includes a region 2 where semiconductor elements are to be produced (hereinafter referred to as element region) and a test pattern 3 for process evaluation (hereinafter referred to as TEG (Test Element Group)) disposed outside the element region 2. Figure 2 is a sectional view taken along a line 2-2 of figure 1. As shown in figure 2, the TEG 3 is a periodic pattern of stripe-shaped

grooves 11 extending in the [011] direction. Reference numeral 12 designates stripe-shaped ridge portions of the GaAs substrate 1 produced between the grooves 11.

Figures 3(a)-3(c) are sectional views taken along the line 2-2 of figure 1 for explaining a method for evaluating an epitaxial layer growing on the substrate, according to the first embodiment of the present invention. In this first embodiment, a GaAs layer 20 is epitaxially grown on the GaAs substrate 1. Reference numeral 21 designates an incident light on the TEG comprising the alternating stripe-shaped grooves 11 and ridges 12. Reference numeral 22 designates a diffracted light produced by reflection type diffraction of the incident light 21 at a flat portion of the TEG. Reference numeral 23 designates a diffracted light produced by reflection type diffraction of the incident light 21 at a (111)B plane that is formed during the crystal growth on the TEG. Reference numeral 25 designates a normal line perpendicular to the surface of the substrate 1.

A description is given of the evaluation method.

Initially, as illustrated in figure 3(a), a periodic pattern of stripe-shaped grooves 11 extending in the [011] direction is formed on the (100) surface of the GaAs substrate 1 using photolithography and dry etching, whereby a TEG comprising these stripe-shaped grooves 11 and a plurality of stripe-shaped ridges 12 between these grooves 11 is produced. The width (W) and the height (H) of the ridge 12 are adjusted so that the TEG is completely buried in an epitaxially grown layer 20 with a flat surface when the layer 20 attains a desired thickness d.

In the step of figure 3(b), a GaAs epitaxial layer 20 is grown on the GaAs substrate 1 by MOCVD. On the stripe-shaped ridge 12 extending in the [011] direction, the crystal growth proceeds forming (111)B planes on which no crystal grows. In this first embodiment, during the crystal growth process, the TEG is irradiated with light 21, such as laser light, and either or both of the diffracted lights 22 and 23 is/are monitored. The incident light 21 is applied to the TEG in a direction perpendicular to the stripe direction of the TEG, at an incident angle $\theta 1$ with respect to the normal line 25 perpendicular to the surface of the substrate 1. The epitaxial growth is stopped when the stripe-shaped ridges 12 of the TEG are completely buried and the surface of the grown layer 20 becomes flat as shown in figure 3(c), whereby the desired thickness d is obtained.

A description is given of the principle of the above-described evaluation method. Figures 4(a)-4(c) and 5(a)-5(b) are diagrams illustrating reflections of incident light on the TEG at different steps in the epitaxial growth process. Figure 6 is a graph illustrating growth time (T) vs. diffracted light intensity (R) characteristics. In figure 6, a curve A shows a change of the intensity of the diffracted light 22, and a curve B shows a change of the intensity of the diffracted light 23.

Figure 4(a) illustrates reflection of incident light 21 on the surface of the TEG before the epitaxial growth, i.e., at the growth time T = 0 of figure 6. The TEG formed on the GaAs substrate 1 is a reflection type diffraction grating. In figure 4(a), assuming that the width of the ridge 12 be W, the width of the groove 11 be D, and the diffraction angle be $\theta 2$, the diffraction condition of the incident light 21 at the incident angle $\theta 1$ is represented by

$$(D + W) \cdot (\sin\theta 1 + \sin\theta 2) = m\lambda$$

where m is degree.

Therefore, a main peak (m = 0) of the diffracted light 22 is observed in a direction of diffraction angle $\theta 2 = -\theta 1$. The incident angle $\theta 1$ is selected to satisfy the relation

$$|\theta 1| \leq \tan^{-1}(2H/D)$$

so that a high-order component due to multiple reflection at the side surface of the stripe-shaped ridge 12 is quenched.

In addition, the diffracted light intensity R1 of the main peak is given by

$$R1 \sim R0\ W/(D + W)$$

where R0 is the reflected light intensity at the flat surface.

Figure 4(b) illustrates reflection of incident light 21 on the surface of the TEG during the epitaxial growth, at the growth time T1 of figure 6. Since the GaAs epitaxial layer 20 does not grow on the (111)-B plane, the growth proceeds forming a trapezoid portion on each stripe-shaped ridge 12 of the TEG as shown in figure 4(b). The incident light 21 is diffracted at the inclined plane of the trapezoid portion, i.e., the (111)B plane (diffracted light 23). The incident angle $\phi 1$ on the inclined plane and the diffraction angle $\phi 2$ of the main peak have the relation of $\phi 2 = -\phi 1$. Therefore, assuming that the inclination of the inclined plane of the trapezoid portion be χ, the diffracted light 23 is observed in a direction of $\theta 3 = 2\chi - \theta 1$.

Figure 4(c) illustrates reflection of incident light 21 on the TEG during the epitaxial growth, at the growth time T2 of figure 6. The epitaxial growth on the stripe-shaped ridge 12 of the TEG stops when a triangle is formed as shown in figure 4(c). When the triangle is formed, the intensity of the diffracted light 23 in the direction of $\theta 3 = 2\chi - \theta 1$ becomes the maximum. Since the inclination χ of the in-

clined plane of the trapezoid portion, i.e., the inclination of the (111)B plane with respect to the (100) surface of the substrate, is about 54°, the diffracted light intensity R2 at this time in the same direction is given by

$$R2 \sim R0\ W(0.7/\tan\theta 1 + 0.5)/(D + W)$$

In addition, the diffracted light intensity A in the $\theta 2 = -\theta 1$ direction becomes the minimum.

Figure 5(a) illustrates reflection of incident light 21 on the TEG during the epitaxial growth, at the growth time T3 of figure 6. As the triangle portions on the stripe-shaped ridges of the TEG are gradually embedded by the growing GaAs layer 20 as shown in figure 5(a), the diffracted light intensity A in the $\theta 2$ direction increases and the diffracted light intensity B in the $\theta 3$ direction decreases.

Figure 5(b) shows reflection of incident light 21 on the TEG after the epitaxial growth is completed, at the growth time Te of figure 6. When the triangle portions on the stripe-shaped ridges of the TEG are completely embedded in the growing GaAs layer 20, i.e., when the surface of the GaAs layer 20 growing on the TEG becomes flat, the incident light 21 is reflected at the flat surface in the $\theta 2 = -\theta 1$ direction. That is, only the diffracted light 22 remains. Accordingly, the completion of the TEG stripe embedding growth is detected by irradiating the TEG with light at an angle $\theta 1$ and observing the diffracted light intensities in the $-\theta$ direction and the $2\chi - \theta$ direction.

In this first embodiment of the present invention, since diffracted light from the TEG 3 having a relatively large size that is determined according to a desired thickness of an epitaxially grown layer is monitored, an increased signal intensity is obtained compared to the prior art method shown in figure 18 in which diffracted light caused by the atomic layer level unevenness is monitored. Therefore, the growth conditions of the epitaxial layer are detected with high precision, without polarizing the incident light.

A description is given of the width W and the height H of the stripe-shaped ridges 12 of the TEG 3.

As described above, the epitaxial growth on the TEG proceeds forming a triangle portion having (111)B planes on each stripe-shaped ridge of the TEG. Since the angle χ formed between the (111)B plane and the (100) surface of the substrate is about 54°, the thickness of the triangle layer grown on the ridge 12 is about 0.7W. On the other hand, the thickness of the epitaxial layer grown on a region of the substrate 1 other than the TEG region 3 is approximately equal to the thickness of the epitaxial layer grown in the stripe-shaped groove 11 of the TEG. More specifically, the thickness d of the epitaxial layer grown on the substrate 1 other than the TEG region 3 shown in figure 3(c) is approximately equal to the thickness d' of the epitaxial layer grown in the groove 11 shown in figure 5(b). The thickness d' is represented by 0.7W + H.

Accordingly, if a desired thickness of the epitaxial layer is d, the width W and the height H of the stripe-shaped ridge 12 are selected so that the relation of d = 0.7W + H is satisfied, whereby an epitaxial layer with the desired thickness d is grown on the substrate other than the TEG region at the moment when the TEG region is flatly embedded.

As described above, according to the first embodiment of the present invention, the TEG 3 including a plurality of stripe-shaped ridges 12 extending in a prescribed direction is formed on the substrate. The TEG is irradiated with light in a prescribed direction during the epitaxial growth on the substrate, and light diffracted by the TEG is monitored. Therefore, the thickness of the epitaxial layer is evaluated with high precision, without cleaving the substrate.

While in the above-described first embodiment the TEG 3 is formed directly on the surface of the GaAs substrate 1, it may be formed on a semiconductor layer 1a disposed on the substrate 1, as illustrated in figures 21(a)-21(b).

While in the above-described first embodiment the epitaxial growth is carried out by MOCVD, the present invention may be applied to epitaxial growths employing other vapor phase growth methods, such as MBE (Molecular Beam Epitaxy) or CBE (Chemical Beam Epitaxy).

Further, while in the above-described first embodiment the stripe-shaped ridges 12 of the TEG 3 are formed in rectangle with dry etching, these ridges may be formed in reverse-mesa shape using wet etching. Also in this case, the same effects as described above are achieved.

Figure 7 is a schematic diagram illustrating an epitaxial growth apparatus employed for the above-described evaluation process according to the first embodiment of the present invention. In figure 7, reference numeral 31 designates a reaction furnace containing a substrate holder 32. The GaAs substrate 1 including the TEG 3 shown in figure 1 is disposed on the substrate holder 32. An incident light 21 is introduced into the furnace 31 through an entrance window 33. The incident light 21 is diffracted by the TEG 3 on the substrate 1. The diffracted light 22 is taken out of the furnace from an exit window 34. Reference numeral 35 designates a laser light source and reference numeral 36 designates a photodetector. The TEG 3 on the substrate 1, the entrance window 33, and the exit window 34 are arranged so that the incident angle $\theta 1$ of the incident light 21 and the diffraction angle

$\theta 2$ of the diffracted light 22 have the relation of $\theta 2 = -\theta 1$ and the incident light 21 is perpendicular to the stripe direction of the TEG 3. In a case where the GaAs substrate 1 is rotated during the epitaxial growth process, the rotation of the GaAs substrate 1 should be synchronized with the switching of the incident light 21 so that the evaluation is carried out only at the moment when the incident light 21 is perpendicular to the stripe direction of the TEG 3. Further, the entrance window 33 and the exit window 34 must be flat so that the incident light 21 and the diffracted light 22 are not broadened. Alternatively, those windows 33 and 34 may be convex lenses that condense the incident light 21 and the diffracted light 22, respectively. During the epitaxial growth, a carrier gas, such as H_2, is flown in the furnace to prevent the inner wall of the furnace from being clouded.

Using the above-described epitaxial growth apparatus, the diffracted light 22 from the TEG 3 is monitored during the epitaxial growth process, and the thickness of the epitaxially growing layer is evaluated with high precision, whereby production yield of semiconductor devices is improved.

In the apparatus shown in figure 7, only the diffracted light 22 in the $\theta 2$ direction, i.e., diffracted light at the flat surface of the TEG 3, is monitored through the exit window 34. However, the exit window may be positioned so that the diffracted light 23 in the $\theta 3$ direction, i.e., diffracted light at the sloping surface of the TEG 3, is monitored. Alternatively, two exit windows may be provided so that both of the diffracted lights 22 and 23 are monitored.

A description is given of a second embodiment of the present invention in which the above-described evaluation method is applied to an epitaxial growth process in a production of a semiconductor laser.

Figure 8 is a perspective view, partially in section, illustrating an InP semiconductor laser having a diffraction grating. In the figure, reference numeral 40 designates a p type InP substrate having a (100) surface orientation. A p type InP lower cladding layer 41 is disposed on the substrate 40. An undoped InGaAsP active layer 42 is disposed on the lower cladding layer 41. An n type InP barrier layer 43 is disposed on the active layer 42. A plurality of stripe-shaped n type InGaAsP layers 44 producing a diffraction grating are disposed on the InP barrier layer 43. These stripe-shaped InGaAsP layers 44 are periodically arranged parallel to each other and perpendicular to the resonator length direction of the laser. A first n type InP upper cladding layer 45 is disposed on the n type InGaAsP layers 44 and on the n type InP barrier layer 43. The first upper cladding layer 45, the n type InGaAsP layers 44, the barrier layer 43, the active layer 42, and the lower cladding layer 41 are formed in a stripe-shaped mesa by etching. A p type InP layer 46 is disposed on part of the substrate 40, contacting the opposite sides of the mesa. An n type InP layer 47 is disposed on parts of the p type InP layer 46. An additional p type InP layer 48 is disposed on the n type InP layer 47 and part of the p type InP layer 46. A second n type InP upper cladding layer 49 is disposed on the p type InP layer 48 as well as on the first upper cladding layer 45. An n type InGaAsP contact layer 50 is disposed on the second upper cladding layer 49. An insulating film, such as SiO_2, including a window opposite the stripe-shaped mesa is disposed on the top and side surfaces of the laser structure. A p side electrode 52 is disposed on the rear surface of the substrate 40 and an n side electrode 53 is disposed on the insulating film 51, contacting the InGaAsP contact layer 50 through the window in that insulating film 51.

Figures 9(a)-9(c) are sectional views illustrating process steps in a method for evaluating an epitaxially grown layer according to the second embodiment of the present invention.

A description is given of the evaluation method. Initially, as illustrated in figure 9(a), the p type InP cladding layer 41, the undoped InGaAsP active layer 42, the n type InP barrier layer 43, and the n type InGaAsP layer 44 are successively grown on the (100) surface of the p type InP substrate 40. Thereafter, a mask pattern for selective etching is formed on the n type InGaAsP layer 44 using photolithographic techniques, and the n type InGaAsP layer 44 is patterned in a plurality of stripe-shaped ridges which are periodically arranged parallel to each other and perpendicular to what becomes the resonator length direction of the laser, preferably by wet etching using HBr system etchant, whereby a diffraction grating is produced. If the stripe-shaped ridges of the n type InGaAsP layer 44 are formed in the [011] direction, each ridge has a trapezoid section as shown in figure 9-(b).

Thereafter, the n type InP cladding layer 45 is grown on the n type InP barrier layer 43 and on the diffraction grating 44, preferably by MOCVD. During the MOCVD growth, the diffraction grating 44 is irradiated with light 21, such as laser light, and diffracted light 22 is monitored, whereby the moment when the diffraction grating 44 is completely embedded by the n type InP cladding layer 45 as shown in figure 9(c) is detected. The incident light 21 is applied perpendicularly to the stripe direction of the diffraction grating 44.

In the above-described production process of the semiconductor laser, when the first n type InP upper cladding layer 45 is grown on the diffraction grating comprising the stripe-shaped InGaAsP lay-

ers 44 by vapor phase deposition, the diffraction grating unfavorably gets out of shape due to mass transport in the InGaAsP layers, whereby thickness and amplitude of the diffraction grating are reduced, resulting in a difficulty in controlling the coupling coefficient that shows the intensity of distributed feedback applied to light. The unwanted mass transport is suppressed by decreasing the growth temperature of the first n type InP upper cladding layer 45. However, since low temperature growth does not provide a high-quality crystalline layer, it is not desired that the entire first upper cladding layer 45 be formed at a low temperature.

Employing the evaluation method according to this second embodiment of the present invention, the moment when the diffraction grating comprising the stripe-shaped n type InGaAsP layers 44 is completely embedded is easily detected. Therefore, the first n type InP upper cladding layer 45 is grown at a relatively low temperature until this moment and, thereafter, it is grown at a relatively high temperature, whereby the mass transport is suppressed as well as the crystal quality of the first upper cladding layer 45 is improved.

As described above, according to the second embodiment of the present invention, the n type InGaAsP layer 44 is patterned in a plurality of stripe-shaped parallel ridges to form a diffraction grating, and the first n type InP upper cladding layer 45 is epitaxially grown thereon. During the epitaxial growth, the stripe-shaped ridges of the diffraction grating are irradiated with light, and light diffracted by the stripe-shaped ridges is monitored, whereby the moment when the stripe-shaped ridges are completely embedded in the first n type InP upper cladding layer 45 is detected. Therefore, the growth conditions can be controlled with high precision, improving the crystal quality and structure controllability.

Figures 10(a)-10(c) are sectional views for explaining a method for evaluating an epitaxially growing layer in accordance with a third embodiment of the present invention. In these figures, reference numeral 55 designates a GaAs substrate. A first TEG 56 and a second TEG 57 are formed at prescribed positions on the surface of the GaAs substrate 55. The first TEG 56 includes a plurality of stripe-shaped portions of the substrate 55, each having a width W1 and a height H1. The second TEG 57 includes a plurality of stripe-shaped portions of the substrate 55, each having a width W2 and a height H2. A first epitaxial layer 58 is grown on the substrate 55, and a second epitaxial layer 59 is grown on the first epitaxial layer 58.

The widths W_1 and W_2 have a relation of $W_1 < W_2$, and the heights H_1 and H_2 have a relation of $H_1 = H_2$.

Initially, the first epitaxial layer 58 is grown on the substrate 55 including the first and second TEG's 56 and 57. In the step of figure 10(a), the epitaxial growth proceeds forming (111)B planes on the stripe-shaped ridges of the respective TEG's 56 and 57, as described in the first embodiment. During the epitaxial growth, the TEG's 56 and 57 are irradiated with light, and diffracted lights from the respective TEG's are monitored.

In the step of figure 10(b), the moment when only the first TEG 56 is flatly embedded in the first epitaxial layer 58 is detected by the diffracted light from the first TEG 56, and the growth of the first epitaxial layer 58 is stopped at this moment. Thus, a first epitaxial layer 58 having a desired thickness d_1 approximately equal to $0.7 W_1 + H_1$ is formed on a region of the substrate 55 where the TEG's 56 and 57 are absent. Thereafter, a second epitaxial layer 59 is grown on the first epitaxial layer 58. In the step of figure 10(c), the moment when the second TEG 57 is flatly embedded is detected by the diffracted light from the second TEG 57, and the growth of the second epitaxial layer 59 is stopped at this moment. Thus, a second epitaxial layer 59 having a desired thickness d_2 approximately equal to $(0.7W_2 + H_2) - (0.7W_1 + H_1)$ is formed on the first epitaxial layer 58 in the region where the TEG's 56 and 57 are absent.

Accordingly, the first and second epitaxial layers 58 and 59 are grown to the desired thicknesses with high precision by appropriately selecting the widths W_1 and W_2 and the heights H_1 and H_2 of the stripe-shaped ridges of the first and second TEG's 56 and 57, respectively.

While in the above-described third embodiment the first and second TEG's, which are different in size, are formed on the substrate and the thicknesses of the first and second epitaxial layers grown on the substrate are evaluated, three or more TEG's may be formed to evaluate thicknesses of three or more epitaxial layers.

The evaluation method of the present invention is applied to epitaxial growth on a GaAs substrate in the above-described first and third embodiments and to production of an InP laser in the above-described second embodiment. However, the evaluation method of the present invention may be applied to epitaxial growth of other materials.

Figure 11 is a perspective view of a substrate including a TEG for evaluating an epitaxial layer grown on the substrate, in accordance with a fourth embodiment of the present invention. In figure 11, reference numeral 61 designates a GaAs substrate having a (100) surface orientation, numeral 62 designates a region where semiconductor elements are formed (hereinafter referred to as element region), and numeral 63 designates a TEG formed on a region of the substrate 61 other than the element

region 62. Figure 12 is an enlarged view of the TEG 63 of figure 11. In figure 12, reference numeral 65 designates a mask pattern comprising a pair of SiO_2 films, and numeral 66 designates an opening of the mask pattern 65.

Figure 14 is a sectional view taken along a line 14-14 of figure 12, illustrating semiconductor layers including an AlGaAs MQW layer, which are epitaxially grown on the TEG 63 of the substrate 61. In the figure, a first AlGaAs layer 71 is grown on the GaAs substrate 61, an AlGaAs MQW layer 72 is grown on the first AlGaAs layer 71, and a second AlGaAs layer 73 is grown on the MQW layer 72.

A description is given of the evaluation method.

Initially, an SiO_2 mask pattern 65 having an opening 66 is formed on the TEG region 63 of the GaAs substrate 61 by vapor deposition and photolithographic techniques. The ratio of the width of the opening 66 to the width of the mask pattern 65 (hereinafter referred to as opening ratio) is gradually varied as shown in figure 12. The width of the SiO_2 mask pattern 65 is selected so that no polycrystalline film is deposited on the mask pattern in the subsequent crystal growth process. For example, it is less than 10 μm. Thereafter, the first AlGaAs layer 71, the AlGaAs MQW layer 72, and the second AlGaAs layer 73 are grown on the GaAs substrate 61 including the TEG 63, preferably by MOCVD.

Figure 13 is a graph illustrating the relationship between the growth rate and the opening ratio of the SiO_2 mask pattern. As shown in figure 13, on the substrate 61 exposed in the opening 66 of the SiO_2 mask pattern 65, the thicknesses of those grown layers are increased as the opening ratio is reduced because atoms reaching the SiO_2 mask pattern migrate toward the substrate 61 exposed in the opening 66. That is, as shown in figure 14, the thicknesses of the grown layers are greater at a position Z-Z' where the opening ratio of the mask pattern is relatively small than at a position Y-Y' where the opening ratio is relatively large. The rate of the increase in the thickness is in proportion to the rate of the decrease in the opening ratio of the mask pattern. In addition, the PL peak wavelength of the AlGaAs MQW layer shifts toward longer wavelength side with an increase in the thickness of the well layer. Therefore, PL wavelengths at different positions of the AlGaAs MQW layer with different opening ratios of the mask pattern 65 make a distribution.

Figure 15 is a graph illustrating PL peak wavelength vs. well layer thickness characteristics obtained from a wave function of a quantum well structure. In figure 15, the continuous line shows PL peak wavelengths at different well layer thicknesses (standard thicknesses) when the Al composition ratio is 0.1 (standard Al composition ratio). The upper and lower broken lines show PL peak wavelengths at different well layer thicknesses that are by 10 % thicker and thinner than the standard thicknesses, respectively, with the standard Al composition ratio. The upper and lower alternate long and short dash lines shows PL peak wavelengths at the standard well layer thicknesses when the Al composition ratio is by 0.01 decreased and increased from the standard Al composition ratio, respectively. As shown in figure 15, the variation in the distribution of the PL peak wavelengths due to the variation in the well layer thickness shown by the broken line is different from the variation in the distribution of the PL peak wavelengths due to the variation in the Al composition ratio shown by the alternate long and short dash line. That is, the PL peak wavelengths are sensitive to the variation in the well layer thickness and the variation in the Al composition ratio.

On the other hand, since the difference in thicknesses of the AlGaAs MQW layer between two positions of the opening 66 of the mask pattern 65 with different opening ratios is obtained from the relationship between the growth rate and the opening ratio shown in figure 13, when PL wavelengths at different positions with different opening ratios of the SiO_2 mask pattern 65 are measured, a distribution of PL peak wavelengths to the rate of change in the thickness of the well layer included in the epitaxially grown AlGaAs MQW layer is obtained.

Thus obtained distribution of PL peak wavelengths is compared to the standard distribution shown in figure 15 which is obtained from the wave function of the quantum well structure. That is, the distribution curve is fitted with theoretical curves obtained by calculations in which the Al composition ratio and the well layer thickness are varied, whereby the thickness and the Al composition of the AlGaAs MQW layer are precisely evaluated.

As described above, in this fourth embodiment of the present invention, the insulating mask pattern 65 with the continuously varied opening ratio is formed on the substrate 61, and the semiconductor layers including the AlGaAs MQW layer 72 are epitaxially grown on the substrate by vapor phase deposition. Thereafter, PL peak wavelengths of the AlGaAs MQW layer grown in the opening 66 of the mask pattern 65 are measured at different positions, and the measured values are compared to the theoretical curves with respect to a standard quantum well structure, whereby the thickness and the Al composition of the AlGaAs MQW layer are evaluated. Therefore, the evaluation of the thickness and the Al composition of the AlGaAs MQW layer is performed with high precision without cleaving the wafer.

While in the above-described fourth embodiment the opening ratio of the SiO_2 mask pattern 65 is continuously varied as shown in figure 12, it may be varied in steps as shown in figure 16. Also in this case, the same effects as described above are achieved.

Claims

1. A method for evaluating thickness of a semiconductor layer (20) epitaxially growing on a first surface of a substrate (1) or on a semiconductor layer (1a) formed on the first surface of the substrate (figures 3(a)-3(c)), comprising:

   forming a plurality of stripe-shaped ridges (12) extending in a prescribed direction on the first surface of the substrate (1) or on the semiconductor layer (1a); and

   epitaxially growing a semiconductor layer (20) on the first surface of the substrate (1) or the semiconductor layer (1a) including the stripe-shaped ridges (12) while irradiating the stripe-shaped ridges (12) with light (21) and monitoring diffracted light (22,23) from the stripe-shaped ridges (12) to evaluate the thickness of the epitaxially growing semiconductor layer (20).

2. The method of claim 1 including forming the stripe-shaped ridges (12) in a direction selected so that a semiconductor layer (20) having a triangle section and side surfaces on which the epitaxial growth does not proceed is grown on each of the stripe-shaped ridges (12).

3. The method of claim 1 or 2 including forming the stripe-shaped ridges (12), each having a width W and a height H, so that the width W and the height H of the ridge and a desired thickness d of the epitaxially grown layer have a relation of $d = 0.7W + H$.

4. The method of one of claims 1 to 3 including forming the stripe-shaped ridges (12) on a (100) surface of the substrate (1) and in a [011] direction.

5. The method of one of claims 1 to 4 including epitaxially growing the semiconductor layer (20) while irradiating the stripe-shaped ridges (12) with light in a direction perpendicular to the stripe direction of the ridges (12).

6. The method of one of claims 1 to 5 (figures 9-(a)-9(c)) wherein said stripe-shaped ridges are stripe-shaped first semiconductor layers (44) which are formed in a fabrication process of a semiconductor laser with a diffraction grating in which said stripe-shaped first semiconductor layers (44) are embedded in a semiconductor region in the vicinity of an active layer (42) and periodically arranged parallel to each other and perpendicular to what becomes the resonator length direction of the semiconductor laser, and thickness of a second semiconductor layer (45) epitaxially growing on the stripe-shaped first semiconductor layers (44) are evaluated.

7. A method of producing a semiconductor laser including a diffraction grating (figures 9(a)-9(c)-) including:

   preparing a semiconductor substrate (40) of a first conductivity type having a (100) surface orientation;

   successively growing a first conductivity type lower cladding layer (41), an active layer (42), a barrier layer of a second conductivity type (43), opposite the first conductivity type, and a second conductivity type semiconductor layer (44) on the (100) surface of the substrate;

   forming the second conductivity type semiconductor layer (44) in a periodic pattern of stripe-shaped ridges extending in a [011] direction and arranged parallel to each other and perpendicular to what becomes the resonator length direction of the semiconductor laser;

   epitaxially growing a second conductivity type upper cladding layer (45) on the barrier layer (43) and on the stripe-shaped ridges (44) while irradiating the stripe-shaped ridges (44) with light (20) and monitoring diffracted light (21) from the stripe-shaped ridges (44) to evaluate the thickness of the epitaxially growing upper cladding layer (45); and

   forming first and second electrodes on the substrate and on the upper cladding layer, respectively.

8. A test pattern (3) for process evaluation (figures 1 and 2) formed on a part of a first surface of a substrate (1) and used for evaluating a semiconductor layer epitaxially growing on the first surface of the substrate, comprising a plurality of stripe-shaped ridges (12) extending in a direction selected so that a semiconductor layer having a triangle section and inclined side surfaces on which the epitaxial growth does not proceed is grown on each of the stripe-shaped ridges (12), and each ridge having a width W and a height H that satisfy a relation of $d = 0.7W + H$ where d is a desired thickness of the semiconductor layer epitaxially grown on the substrate.

9. The test pattern for process evaluation of claim 8 wherein said first surface of the substrate is a (100) surface and said direction of the stripe-shaped ridges is a [011] direction.

10. A method for evaluating an epitaxially grown AlGaAs multiple quantum well layer (figures 12,14,16), comprising:

forming an insulating mask pattern (65) having an opening (66) on a part of a substrate (61) on which a plurality of semiconductor layers including the AlGaAs multiple quantum well layer are to be grown, wherein the ratio of the width of the opening (66) to the width of the insulating mask pattern (65) being varied continuously or in steps;

epitaxially growing a plurality of semiconductor layers including the AlGaAs multiple quantum well layer (72) on the substrate (61) including the insulating mask pattern (65) using a vapor phase growth method; and

measuring PL peak wavelengths of the AlGaAs multiple quantum well layer (72) grown in the opening (66) of the insulating mask pattern (65) at different positions with different opening ratios of the insulating mask pattern (65), and comparing the measured values with theoretical curves obtained with respect to a standard quantum well structure to evaluate the thickness and the Al composition of the AlGaAs multiple quantum well layer (72).

Fig.1

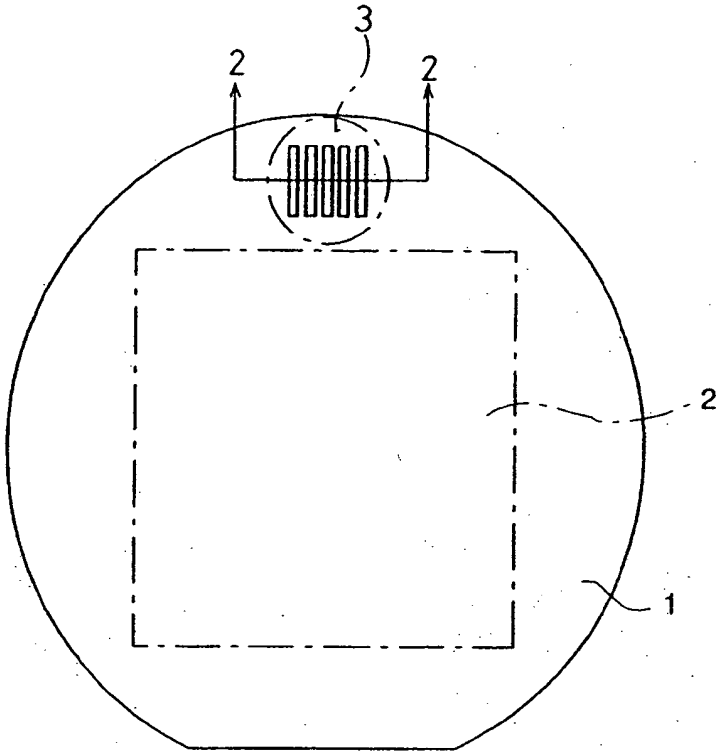


Fig.2

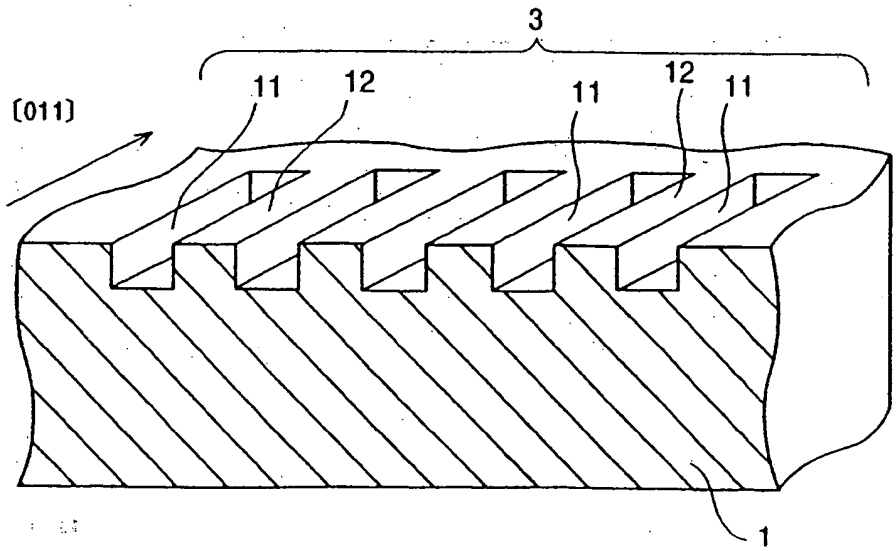


Fig.3 (a)

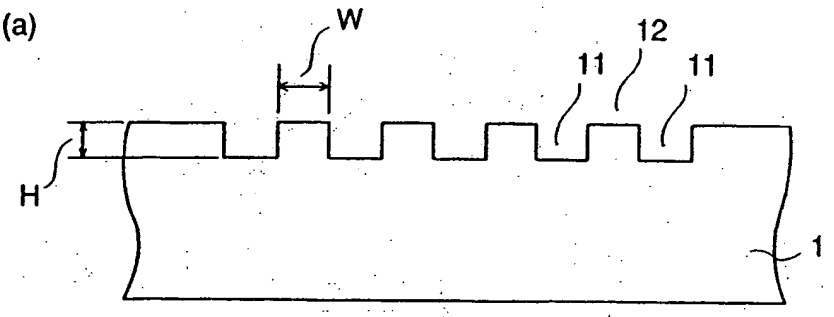


Fig.3 (b)

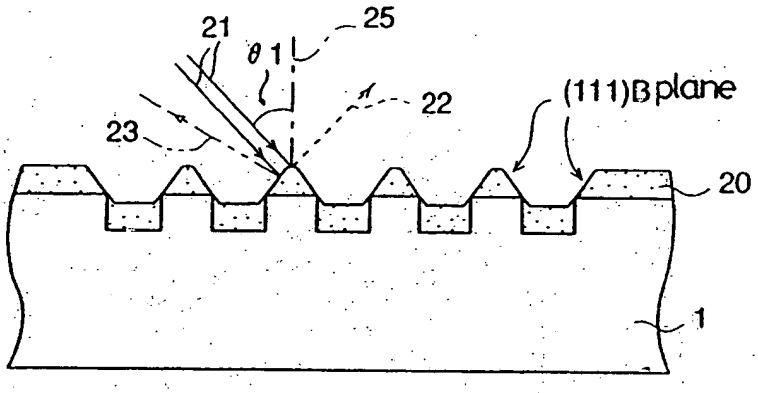


Fig.3 (c)

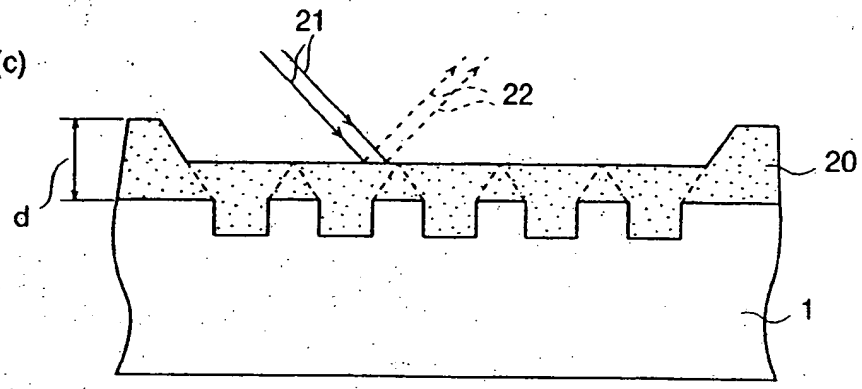


Fig.4 (a)

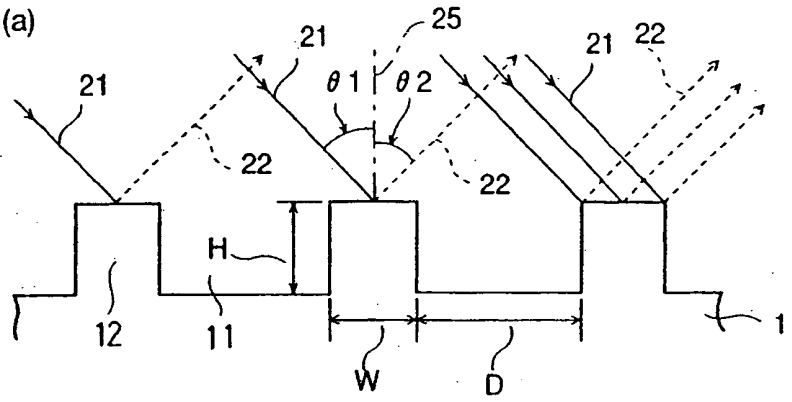


Fig.4 (b)

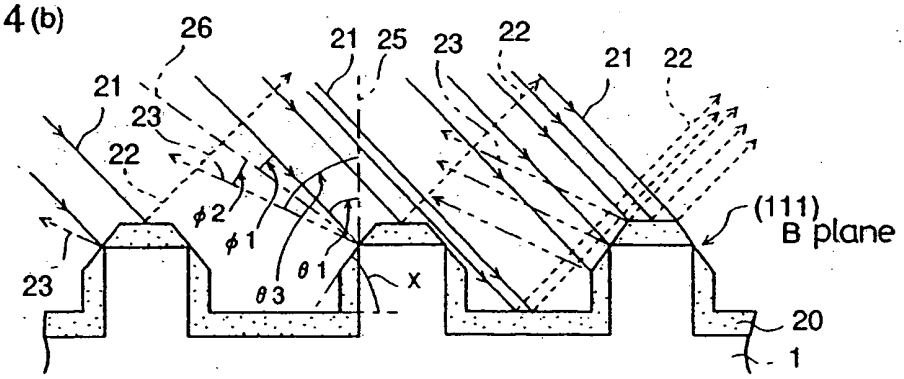


Fig.4 (c)

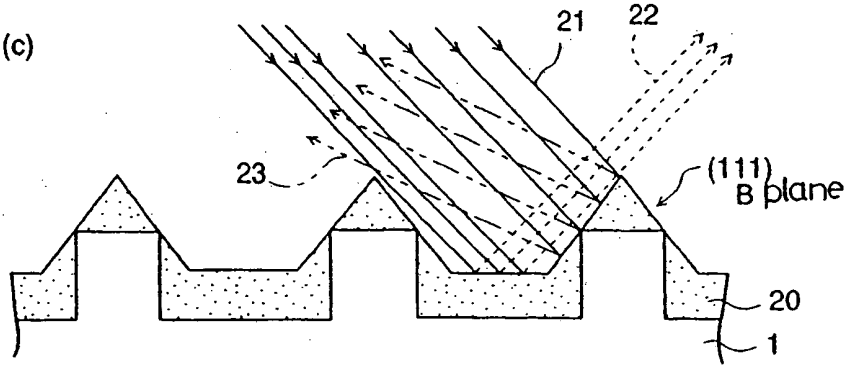


Fig.5 (a)

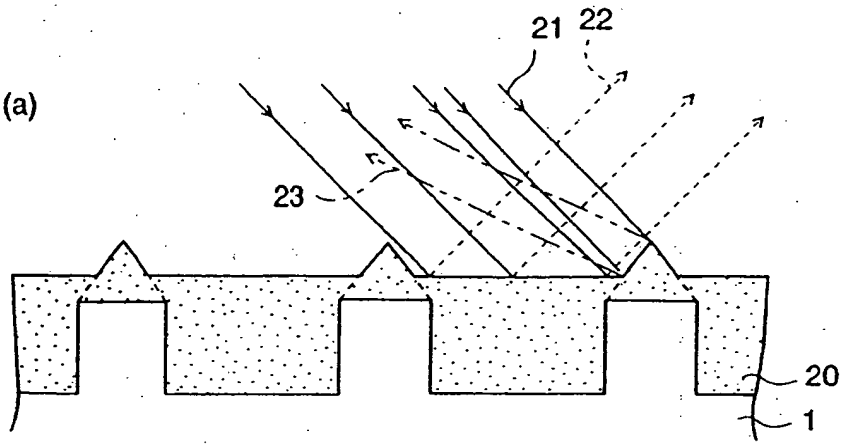


Fig.5 (b)

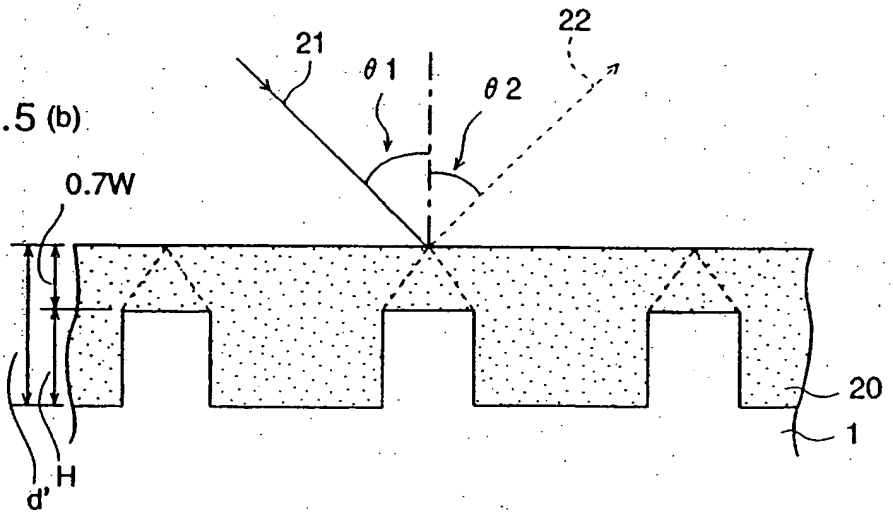


Fig.6

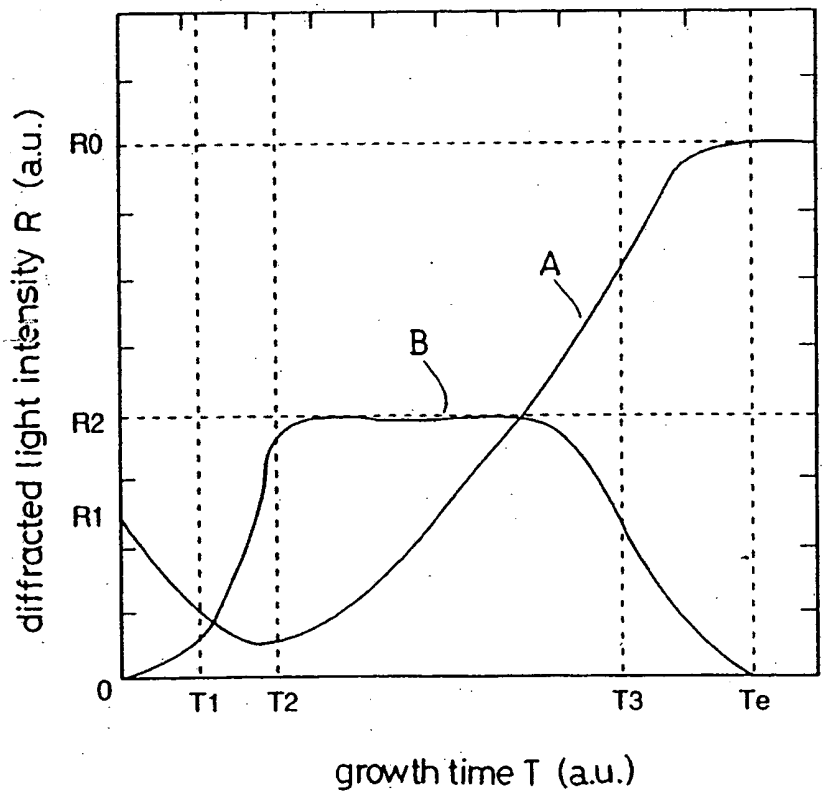

diffracted light intensity R (a.u.)
R0
R2
R1
0
A
B
T1
T2
T3
Te
growth time T (a.u.)

Fig.7

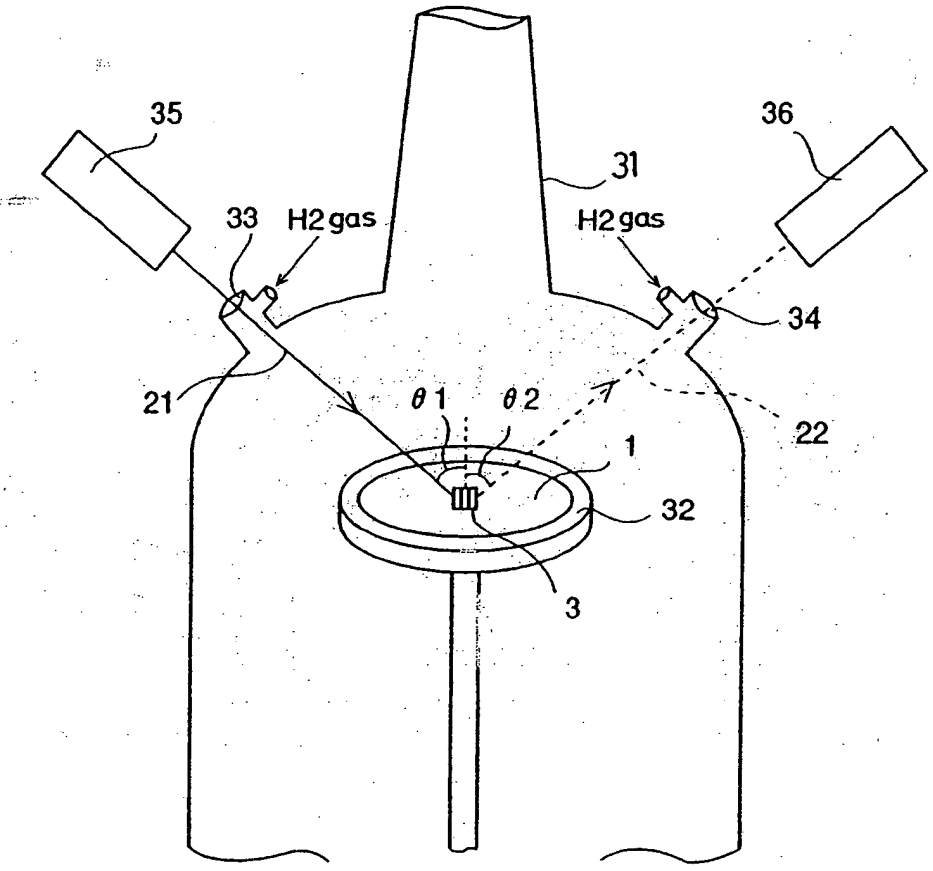


Fig.8

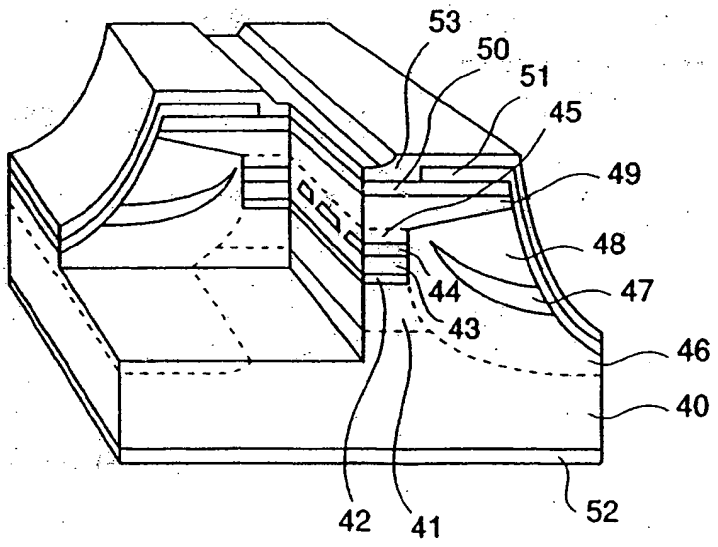


Fig.9 (a)

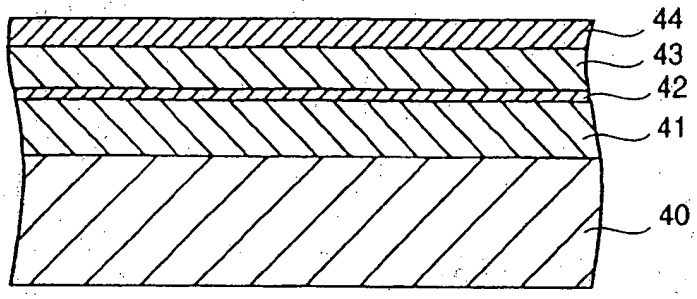


Fig.9 (b)

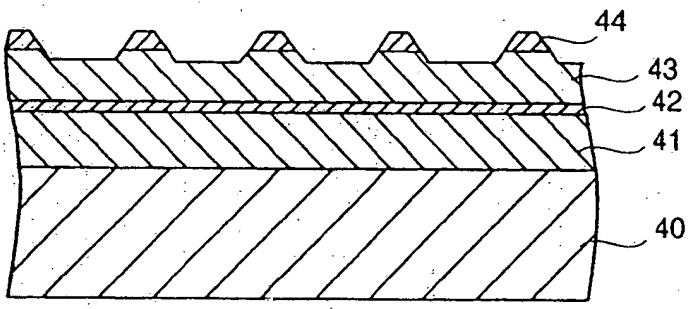
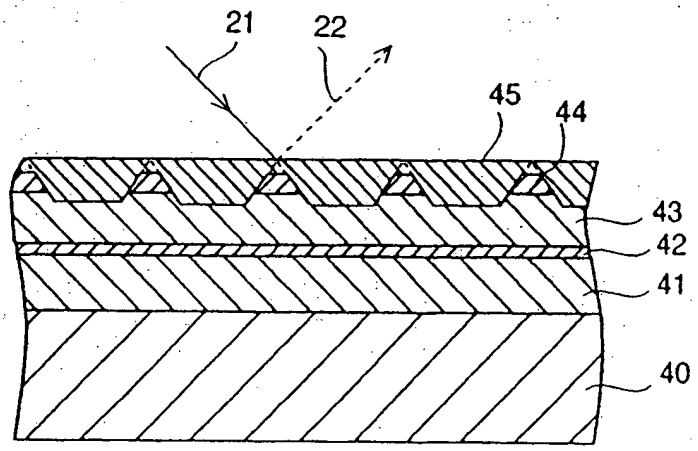


Fig.9 (c)



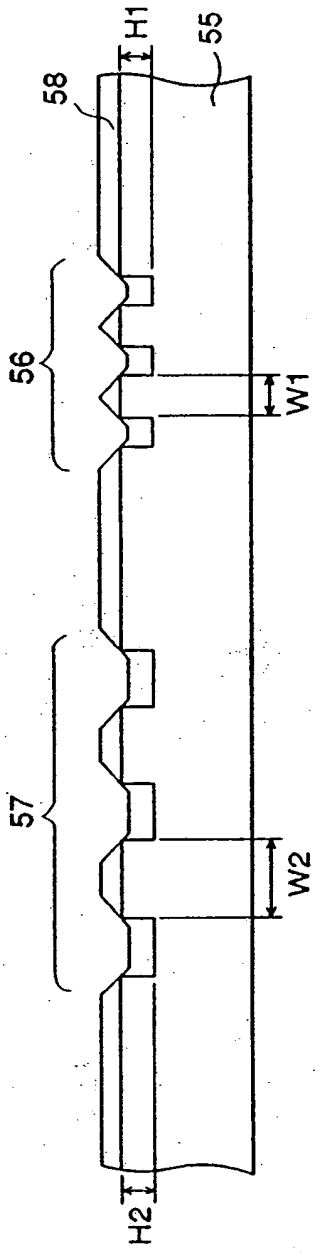


Fig.10(a)

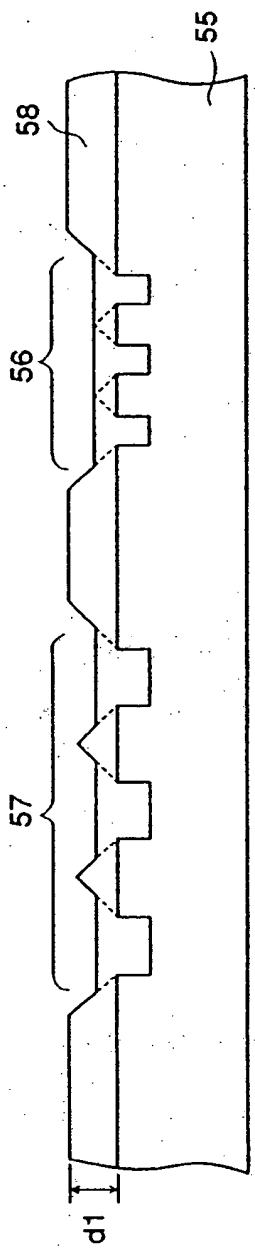


Fig.10(b)

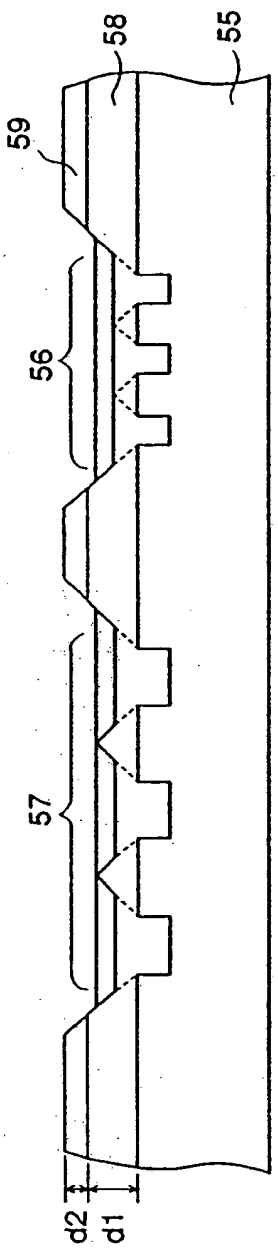


Fig.10(c)

Fig.11

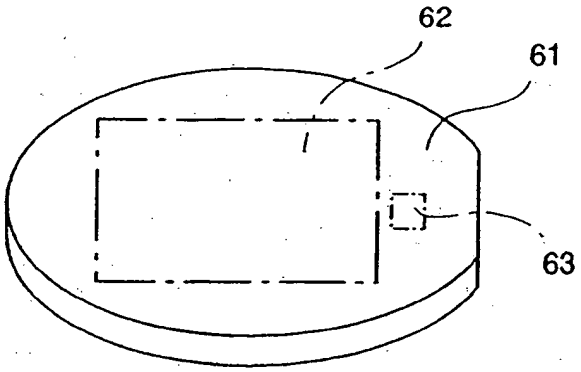


Fig.12

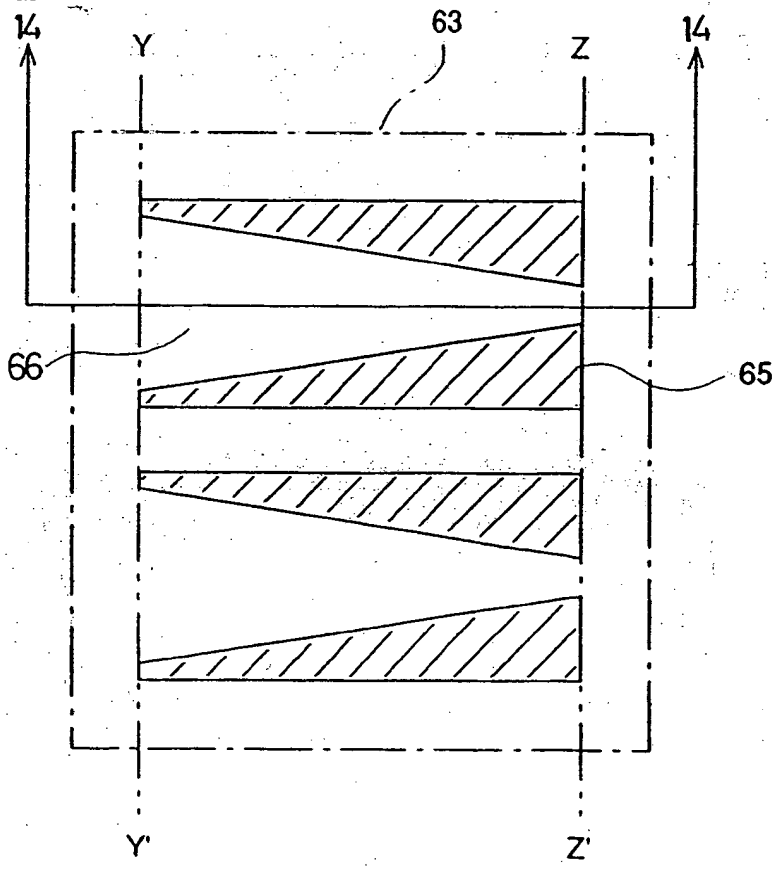


Fig.13

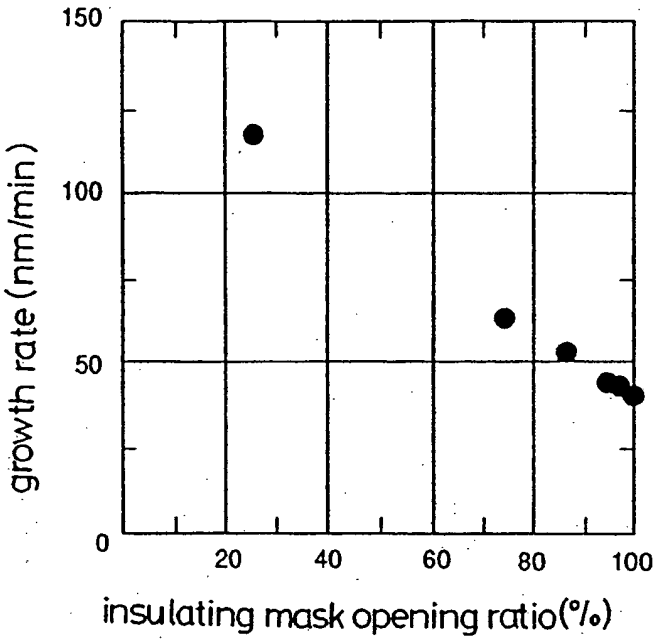

150
100
50
0
20
40
60
80
100
growth rate (nm/min)
insulating mask opening ratio(%)

Fig.14

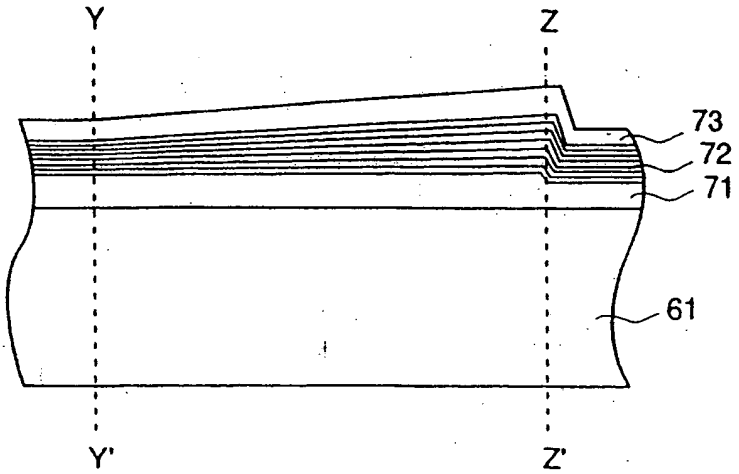

Y
Z
73
72
71
61
Y'
Z'

Fig.15

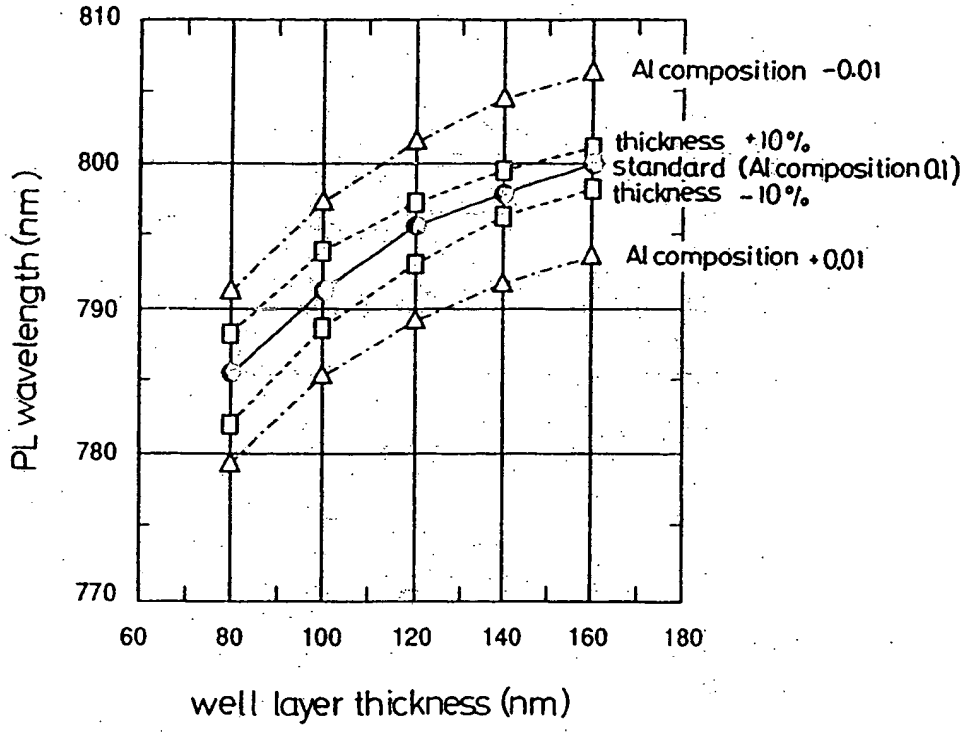
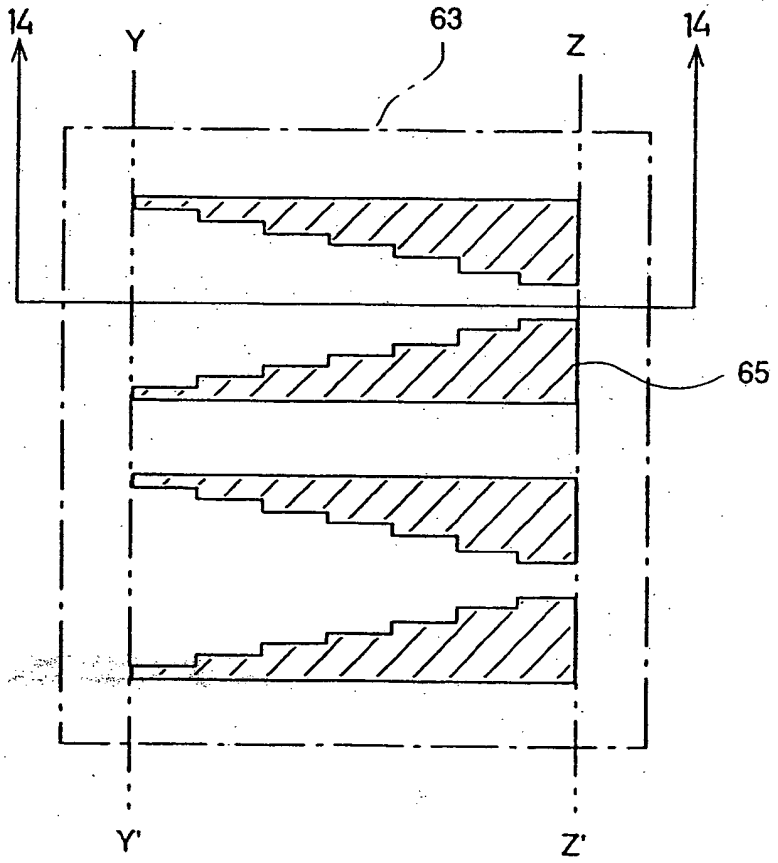

810
800
790
780
770
PL wavelength (nm)
60
80
100
120
140
160
180
well layer thickness (nm)
Al composition -0.01
thickness +10%
standard (Al composition 0.1)
thickness -10%
Al composition +0.01

Fig.16



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Prüfungsantrag gem. § 44 PatG ist gestellt

(54) Verfahren zur Herstellung einer dreidimensionalen integrierten Schaltung

(57) Die Erfindung betrifft ein Verfahren zur Herstellung einer dreidimensionalen integrierten Schaltung.
Beim Zusammenfügen von Substraten, die eine Vielzahl von identischen Bausteinen, den sog. Chips, enthalten, ergibt sich die resultierende Ausbeute eines mehrlagigen Systems aus dem Produkt der Einzelausbeuten. Dies führt dazu, daß die Ausbeute eines mehrere Bauelementeebenen umfassenden Systems nach dem bekannten Verfahren drastisch abnimmt.
Beim erfindungsgemäßen Verfahren werden zwei fertig prozessierte Substrate miteinander verbunden. Vorher wird jedoch das obere Substrat einem Funktionstest unterzogen, mit dem die intakten Chips des Substrates selektiert werden. Anschließend wird dieses Substrat von der Rückseite her gedünnt, in einzelne Chips zerlegt und nur selektierte, intakte Chips auf das, mit einer Haftschicht versehene, untere Substrat justiert aufgebracht.
Mit dem erfindungsgemäßen Verfahren werden die Ausbeute bei der Herstellung dreidimensionaler integrierter Schaltungen deutlich gesteigert und die Herstellungskosten gesenkt.

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Die folgenden Angaben sind den vom Anmelder eingereichten Unterlagen entnommen

Beschreibung

Die Erfindung betrifft ein Verfahren zur Herstellung einer dreidimensionalen integrierten Schaltung. Unter dreidimensionaler Integration versteht man die vertikale Verbindung von Bauelementen, die mittels Planartechnik hergestellt wurden. Die Vorteile eines dreidimensional integrierten mikroelektronischen Systems sind u. a. die bei gleichen Designregeln erreichbaren höheren Packungsdichten und Schaltgeschwindigkeiten gegenüber zweidimensionalen Systemen. Letzteres ist zum einen bedingt durch kürzere Leitungswege zwischen den einzelnen Bauelementen oder Schaltungen, zum anderen durch die Möglichkeit der parallelen Informationsverarbeitung. Die Steigerung der Leistungsfähigkeit des Systems ist bei Realisierung einer Verbindungstechnik mit örtlich frei wählbaren höchstintegrierbaren vertikalen Kontakten optimal.

Zur Herstellung dreidimensionaler Schaltungsanordnungen mit frei wählbaren vertikalen Kontakten sind folgende Verfahren bekannt:

Y. Akasaka, Proc. IEEE 74 (1986) 1703, schlägt vor, auf eine fertig prozessierte Bauelementeschicht polykristallines Silizium abzuscheiden und zu rekristallisieren, so daß in der rekristallisierten Schicht weitere Bauelemente gefertigt werden können. Nachteile dieser Methode sind die ausbeutereduzierende Degradation der Bauelemente in der unteren Ebene durch die hohe thermische Belastung beim Rekristallisierungsprozeß, sowie die notwendigerweise serielle Prozessierung des Gesamtsystems. Letzteres bedingt zum einen entsprechend lange Durchlaufzeiten bei der Fertigung und hat zum anderen eine Ausbeuteminderung durch Aufsummierung der prozeßbedingten Ausfälle zur Folge. Beides erhöht die Fertigungskosten beträchtlich gegenüber einer Prozessierung der einzelnen Ebenen getrennt voneinander in verschiedenen Substraten.

Aus Y. Hayashi et al., Proc. 8th Int. Workshop on Future Electron Devices, 1990, p. 85, ist es bekannt, zunächst die einzelnen Bauelementeebenen getrennt voneinander in verschiedenen Substraten herzustellen. Anschließend werden die Substrate auf wenige Mikrometer gedünnt, mit Vorder- und Rückseitenkontakten versehen und mittels eines Bondverfahrens vertikal verbunden. Für die Bereitstellung der Vorder- und Rückseitenkontakte sind jedoch Sonderprozesse notwendig sind, die in der Standard-Halbleiterfertigung (CMOS) nicht vorgesehen sind, nämlich MOS-inkompatible Materialien (z. B. Gold) und Rückseitenstrukturierung des Substrates.

Ein wesentlicher Nachteil der bisher genannten Verfahren ist dadurch bedingt, daß die in der Siliziumtechnologie zur Verfügung stehenden Geräte nur eine Bearbeitung (Prozessierung) von scheibenförmigen Substraten, den sog. Wafern, zulassen. Eine Prozessierung davon verschiedener Substrate, insbesondere von einzelnen Chips, ist nur in experimentellen Versuchsanlagen möglich, jedoch nicht im Rahmen einer industriellen Fertigung mit den geforderten hohen Ausbeuten.

Beim Zusammenfügen von Substraten, die eine Vielzahl von identischen Bausteinen, den sog. Chips, enthalten, ergibt sich die resultierende Ausbeute eines mehrlagigen Systems aus dem Produkt der Einzelausbeuten. Dies führt dazu, daß die Ausbeute eines mehrere Bauelementeebenen umfassenden Systems nach den bekannten Verfahren drastisch abnimmt. So erhält man bei einer Ausbeute einer Einzelebene von 80% bei einem Gesamtsystem aus 10 Ebenen nur mehr eine resultierende Gesamtausbeute von etwa 10%, womit ein derartiges System unwirtschaftlich wird und der Einsatz dieser Technik auf wenige spezielle Einsatzfelder beschränkt wird. Die Ausbeute eines Bauelementesubstrates hängt dabei auch von der Art der Schaltungen und des verwendeten Herstellungsprozesses ab. So erzielt man z. B. in der Fertigung von Speicherbausteinen sehr hohe Ausbeuten, während bei Logikbausteinen, wie Mikroprozessoren, eine deutlich geringere Ausbeute erreicht wird. Insbesondere wenn mehrere Arten solcher Schaltungen übereinandergestapelt werden, wird damit die Gesamtausbeute überproportional durch die Schaltungsart mit der geringsten Ausbeute bestimmt.

Der Erfindung liegt die Aufgabe zugrunde, ein Verfahren zur Herstellung einer dreidimensionalen integrierten Schaltung anzugeben, mit dem eine deutliche Ausbeutesteigerung gegenüber bisher bekannten Verfahren erzielt wird.

Diese Aufgabe wird erfindungsgemäß mit dem Verfahren nach Anspruch 1 gelöst. Besondere Ausgestaltungen des Verfahrens sind Gegenstand der Unteransprüche.

In dem erfindungsgemäßen Verfahren werden zwei fertig prozessierte Substrate, die jeweils Schaltungsstrukturen und Metallisierungsebenen enthalten, beispielsweise über eine Haftschicht miteinander verbunden. Die Haftschicht kann hierbei zusätzlich eine passivierende Funktion ausüben (Anspruch 7) und/oder eine Planarisierung der Oberfläche bewirken (Anspruch 8). Dabei wird das obere Substrat (zweites Substrat) vorher einem Funktionstest unterzogen, mit dem die intakten Chips des Substrates selektiert werden. Anschließend wird dieses Substrat von der Rückseite her gedünnt und in einzelne Chips zerlegt. Danach werden nur selektierte, intakte Chips auf das, mit einer Haftschicht versehene, untere Substrat (erstes Substrat) justiert aufgebracht.

Das untere Substrat kann hierbei auch bereits mehrere Bauelementelagen in Form von Bauelementestapeln enthalten. Die Chips des oberen Substrates werden entweder im Rahmen des Verfahrens dem Funktionstest unterzogen (Anspruch 2) oder es wird ein bereits geprüftes Substrat mit getesteten und z. B. markierten defekten Chips bereitgestellt und eingesetzt. Auf das obere Substrat wird schließlich vor dem Dünnen und Zerteilen ein Hilfssubstrat aufgebracht. Statt des Dünnens des oberen Substrates bis nahe an die Bauelementelagen heran kann auch im Falle eines SOI-Substrates der Substratbereich unterhalb der Oxidschicht entfernt werden.

Da auf dem unteren Substrat nun einzelne Chips aufgebracht worden sind, ist keine zusammenhängende Oberfläche mehr vorhanden (Gräben zwischen den Chips), so daß bestimmte Prozeßschritte, insbesondere Photolithographiemodule, nicht mehr mit hoher Ausbeute durchgeführt werden können. Deshalb wird nun vorzugsweise ein Planarisierungsschritt eingefügt (Anspruch 9).

Die Planarisierung kann mit verschiedenen Verfahren durchgeführt werden. Dabei wird zuerst eine Isolationsschicht, wie z. B. Spin-on-Glas oder ein CVD-Oxid, aufgebracht, um die Gräben aufzufüllen. Anschließend wird die Oberfläche eingeebnet, was durch Rückätzen, mechanischem oder chemomechanischem Schleifen erfolgt.

Weitere Prozesse, die nicht auf Chipebene realisierbar sind, können nach dem Planarisierungsschritt problemlos an dem Substrat mit vorselektierten Chips

durchgeführt werden.

Anschließend wird z. B. über Vialöcher (Anspruch 10), die bereits bei der Prozessierung der Einzelsubstrate in die Chips eingebracht wurden und nun bis zu einer Metallisierungsebene des unteren Substrates durchgeätzt werden, die elektrische Verbindung zwischen je einer Metallisierungsebene der oberen und der unteren Schaltungsebene hergestellt. Dabei wird die Photomaske zur Strukturierung auf jeden einzelnen Chip über Justierstrukturen separat justiert, um etwaige Maßabweichungen durch das Aufbringen der einzelnen Chips auszugleichen und eine hohe Justiergenauigkeit zu erreichen.

Danach kann das Substrat, das in der Bauelementeebene nur noch getestete und funktionsfähige Chips enthält, in gängigen Fertigungsanlagen weiter verarbeitet werden.

In gleicher Weise kann nun auch eine weitere Bauelementeebene chipweise aufgebracht werden (Anspruch 3). Hierbei dient der bisher hergestellte Bauelementestapel mit zugehörigem Substrat als neues unteres Substrat. Dabei ist bei diesem Verfahren die Anzahl der Ebenen nicht beschränkt. Außerdem kann nicht nur eine Einzelebene, sondern auch ein bereits aus mehreren Ebenen bestehender Teilstapel chipweise aufgebracht werden.

Als Substrate sind monokristalline Siliziumsubstrate, SOI-Substrate oder Substrate verschiedener Technologiefamilien, wie z. B. III-V-Halbleiter geeignet.

Insgesamt werden bei diesem Verfahren nur bekannte und eingeführte Verfahrensschritte verwendet, so daß keine neuen Prozesse entwickelt werden müssen.

Mit dem erfindungsgemäßen Verfahren werden nur intakte Chips jeweils auf die darunterliegenden Bauelementelagen aufgebracht. Damit wird in vorteilhafter Weise die Abhängigkeit der Ausbeute des Gesamtsystems von der Ausbeute der einzelnen prozessierten Substrate stark verringert. Es können jeweils nur einzelne defekte Chips einer Bauelementelage ausgesondert werden, so daß nicht mehr ganze Bauelementestapel aufgrund einer einzigen defekten Lage unbrauchbar werden. Durch das erfindungsgemäße Verfahren werden somit die Ausbeute bei der Herstellung dreidimensionaler integrierter Schaltungen deutlich gesteigert und die Herstellungskosten gesenkt.

Im folgenden wird die Erfindung anhand der Zeichnungen und eines Ausführungsbeispiels näher erläutert.

Dabei zeigen:

Fig. 1 ein erstes Bauelementesubstrat mit Schaltungsstrukturen und Metallisierungsebenen (unteres Substrat),

Fig. 2 ein zweites Bauelementesubstrat mit Schaltungsstrukturen, Metallisierungsebenen und Vialöchern (oberes Substrat),

Fig. 3 das zweite Bauelementesubstrat mit Haftschicht und Hilfssubstrat,

Fig. 4 das erste Bauelementesubstrat mit einer chipweise aufgebrachten zweiten Bauelementeebene nach Planarisierung der Oberfläche, und

Fig. 5 zwei vertikal verbundene Bauelementeebenen.

Ein erstes Bauelementesubstrat 1 aus z. B. monokristallinem Silizium umfaßt mehrere, nach einem definierten Schema angeordnete, üblicherweise identische Chips 2, die Schaltungsstrukturen 3, wie beispielsweise einen MOS-Transistor, und eine oder mehrere Metallisierungsebenen 4 enthalten, die typischerweise aus Aluminum, einer Aluminiumlegierung oder anderen Materialien, wie Kupfer oder Wolfram, bestehen und zur elektrischen Isolation von einer Oxidschicht 5, die zu Planarisierungszwecken auch mit Bor und/oder Phosphor dotiert sein kann, umgeben sind. Die oberste Metallisierungsebene 4 kann dabei auch von einer Passivierungsschicht 6 aus beispielsweise Siliziumoxid und Siliziumnitrid bedeckt sein. Weiterhin sind Justagestrukturen zum genauen Zusammenfügen mehrerer Ebenen implementiert (in Fig. 1 nicht gezeigt). Unterhalb der Schaltungsstrukturen 3 weist das Substrat eine Dicke von z. B. 625 µm auf. Dieses Bauelementesubstrat stellt das untere Substrat des mehrlagigen Systems dar (Fig. 1).

Ein zweites Bauelementesubstrat 7 umfaßt ebenfalls mehrere, nach einem definierten Schema angeordnete, üblicherweise identische Chips 8, die Schaltungsstrukturen 9, wie beispielsweise einen MOS-Transistor, und eine oder mehrere Metallisierungsebenen 10 enthalten. Dieses Substrat 7 ist im wesentlichen ähnlich aufgebaut wie das erste Bauelementesubstrat 1, die Schaltungsstrukturen 9 sind aber in der Regel von ihrer Funktion her unterschiedlich. Desweiteren weist das zweite Bauelementesubstrat Vialöcher 11 an den Stellen auf, an denen später die elektrische Kontaktierung zu darunterliegenden Schaltungsstrukturen des ersten Substrates erfolgen soll. Die Vialöcher 11 sind so tief, daß sie bis unterhalb der Schicht mit Schaltungsstrukturen 9 reichen (Fig. 2).

Nach Fertigstellung des Bauelementesubstrates 7 wird die Passivierung auf der obersten Metallisierungsebene an bestimmten Meßstellen geöffnet. Danach werden die einzelnen Chips des Substrates einem Funktionstest unterzogen und die defekten Chips gekennzeichnet (z. B. mit einem Tintenstrahl). Anschließend wird erneut eine Passivierungsschicht aufgebracht, um die offenliegenden Meßstellen wieder zu schützen.

Auf die Oberfläche des zweiten Substrates 7 wird ganzflächig eine Haftschicht 12 aus einem organischen Material, wie Polyimid oder Photolack, aufgebracht. Diese Haftschicht 12 mit einer Dicke von typischerweise 1—2 µm kann außerdem eine Planarisierung der Oberfläche bewirken. Auf die Haftschicht 12 wird schließlich ein Hilfssubstrat 13, wie beispielsweise ein Silizium- oder Quarzwafer, geklebt. Das Hilfssubstrat 13 wird als Handlingsubstrat für die weiteren Prozeßschritte verwendet und schützt die Oberfläche des Bauelementesubstrates 7 bei der weiteren Bearbeitung. (Fig. 3).

Danach wird das zweite Bauelementesubstrat 7 durch Ätzen und/oder Schleifen von der Rückseite her bis an die Vialöcher 11 heran gedünnt, so daß die Dicke des Substrates 7 unterhalb der Schaltungsstrukturen 9 nur noch wenige Mikrometer, typischerweise 1—5 µm, beträgt. Dabei hängt die gewählte Restdicke auch von der Art der enthaltenen Schaltungen ab.

Nun wird das zweite Bauelementesubstrat 7 mit dem Handlingsubstrat 13 in einzelne Chips zerteilt. Dies kann dabei mit einem Ätzprozeß, durch Sägen oder mit einem Laser erfolgen. Daraufhin werden die gekennzeichneten, intakten Chips auf das, mit einer Haftschicht 14 versehene, erste Bauelementesubstrat 1 justiert aufgebracht. Die Haftschicht 14 mit einer Dicke von typischerweise 1—2 µm kann dabei eine Planarisierung der Oberfläche bewirken. Anschließend werden die Handlingsubstrate 13 z. B. durch Abätzen oder Abschleifen entfernt und die freiliegende Haftschicht 12 typischerweise mit einem Sauerstoffplasma oder einem Lösungsmittel ganzflächig entfernt. Nach dem Aufkleben der Chips weist die Oberfläche des ersten Substrates nun Gräben zwischen den einzelnen Chips auf, die ein sehr

niedriges Aspektverhältnis besitzen. Durch einen Planarisierungsschritt, in dem die Schicht 15 abgeschieden wird, werden diese Gräben nun aufgefüllt und eine ebene Oberfläche erzeugt. Das erste Bauelementesubstrat 1 mit den beiden Bauelementeebenen läßt sich nun wie ein übliches Siliziumsubstrat mit Standard-Technologiegeräten weiterverarbeiten (Fig. 4).

Danach wird schließlich die vertikale Verbindung 16 zwischen einer Metallisierungsebene 10 der oberen Bauelementeebene (Substrat 7) und einer Metallisierungsebene 4 der unteren Bauelementeebene (Substrat 1) hergestellt. Dazu werden mit einem Photolithographieschritt ein Kontaktloch zu einer Metallisierungsebene 10 der oberen Bauelementeebene und die vorbereiteten Vialöcher 11 bis zu einer Metallisierungsebene 4 der unteren Bauelementeebene geöffnet und durch Metallabscheidung und Strukturierung eine elektrische Verbindung realisiert. Schließlich wird auf die Oberfläche noch eine Passivierungsschicht 17 abgeschieden (Fig. 5).

Die elektrische Kontaktierung kann selbstverständlich auch auf andere Weise realisiert werden, so z. B. bereits beim Aufbringen der Chips auf das untere Substrat mittels vorbereiteter Vorder- und Rückseitenkontakte (vgl. Beschreibungseinleitung: Y. Hayashi et al.).

Patentansprüche

1. Verfahren zur Herstellung einer dreidimensionalen integrierten Schaltung mit folgenden Verfahrensschritten:
   - Bereitstellen eines ersten Substrates (1), das auf einer ersten Seite eine oder mehrere fertigprozessierte Bauelementeebenen (3) enthält, die nebeneinander eine Vielzahl von unabhängigen Bauelementen oder Schaltkreisen aufweisen, wobei Bauelemente oder Schaltkreise mehrerer Bauelementeebenen Bauelementstapel bilden;
   - Bereitstellen eines zweiten Substrates (7), das auf einer zweiten Seite eine oder mehrere fertigprozessierte Bauelementeebenen (9) enthält, die nebeneinander eine Vielzahl von unabhängigen Bauelementen oder Schaltkreisen aufweisen, wobei Bauelemente oder Schaltkreise mehrerer Bauelementeebenen Bauelementstapel bilden, und die Bauelemente, Bauelementstapel oder Schaltkreise zur Unterscheidung funktionsfähiger von nicht funktionsfähigen Bauelementen, Bauelementstapeln oder Schaltkreisen auf ihre Funktionsfähigkeit geprüft sind;
   - Verbinden des zweiten Substrates (7) mit einem Hilfssubstrat (13) auf der zweiten Seite;
   - Dünnen oder Entfernen des zweiten Substrates (7) auf der Seite, die der zweiten Seite gegenüberliegt;
   - Zerteilen des Hilfssubstrates (13) mit den verbundenen Bauelementeebenen zu einzelnen Chips, die jeweils funktionsfähige oder nicht funktionsfähige Bauelemente, Bauelementstapel oder Schaltkreise enthalten;
   - Justiertes Aufbringen von Chips, die funktionsfähige Bauelemente Bauelementstapel oder Schaltkreise enthalten, auf das erste Substrat (1) auf der ersten Seite;
   - Entfernen des Hilfssubstrates (13);
   - Herstellen der elektrischen Kontakte zwischen den Bauelementen, Bauelementstapeln oder Schaltkreisen der aufgebrachten Chips und den Bauelementen, Bauelementstapeln oder Schaltkreisen des ersten Substrates, wobei dieser Verfahrensschritt bereits beim Aufbringen der Chips erfolgen kann.

2. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß das Bereitstellen des zweiten Substrates folgende Verfahrensschritte umfaßt:
   - Bereitstellen eines zweiten Substrates (7), das auf einer zweiten Seite eine oder mehrere fertigprozessierte Bauelementeebenen (9) enthält, die nebeneinander eine Vielzahl von unabhängigen Bauelementen oder Schaltkreisen aufweisen, wobei Bauelemente oder Schaltkreise mehrerer Bauelementeebenen Bauelementstapel bilden, und
   - Funktionstest der einzelnen Bauelemente, Bauelementstapel oder Schaltkreise des zweiten Substrates zur Unterscheidung funktionsfähiger von nicht funktionsfähigen Bauelementen, Bauelementstapeln oder Schaltkreisen.

3. Verfahren nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß zum Aufbau einer dreidimensionalen integrierten Schaltung mit mehr als zwei Bauelementeebenen das Verfahren mehrmals nacheinander durchgeführt wird, wobei als erstes Substrat bei jeder wiederholten Durchführung des Verfahrens das bearbeitete erste Substrat des jeweils vorangehenden Verfahrens verwendet wird.

4. Verfahren nach einem der Ansprüche 1 bis 3, dadurch gekennzeichnet, daß erstes und zweites Substrat jeweils genau eine Bauelementeebene enthalten.

5. Verfahren nach einem der Ansprüche 1 bis 4, dadurch gekennzeichnet, daß das Hilfssubstrat (13) über eine Haftschicht (12) mit dem zweiten Substrat (7) verbunden wird.

6. Verfahren nach einem der Ansprüche 1 bis 5, dadurch gekennzeichnet, daß die Chips mittels einer Haftschicht (14) auf die erste Seite des ersten Substrates (1) aufgebracht werden.

7. Verfahren nach Anspruch 5 oder 6, dadurch gekennzeichnet, daß eine Haftschicht mit passivierenden Eigenschaften verwendet wird.

8. Verfahren nach einem der Ansprüche 5 bis 7 dadurch gekennzeichnet, daß eine Haftschicht verwendet wird, die eine Planarisierung der Oberfläche bewirkt.

9. Verfahren nach einem der Ansprüche 1 bis 8, dadurch gekennzeichnet, daß Gräben, die nach dem justierten Aufbringen der einzelnen Chips zwischen diesen entstehen, planarisiert werden.

10. Verfahren nach einem der Ansprüche 1 bis 9 dadurch gekennzeichnet, daß das Herstellen der elektrischen Kontakte zwischen den Bauelementen, Bauelementstapeln oder Schaltkreisen der aufgebrachten Chips und den Bauelementen, Bauelementstapeln oder Schaltkreisen des ersten Substrates über Kontakt- und/oder Vialöcher (11) erfolgt.

11. Verfahren nach einem der Ansprüche 1 bis 10, dadurch gekennzeichnet, daß das Dünnen des zweiten Substrates (7) mittels Ätzen und/oder Schleifen erfolgt.

12. Verfahren nach einem der Ansprüche 1 bis 11,

dadurch gekennzeichnet, daß ein SOI-Substrat als zweites Substrat (7) verwendet wird.

Hierzu 2 Seite(n) Zeichnungen

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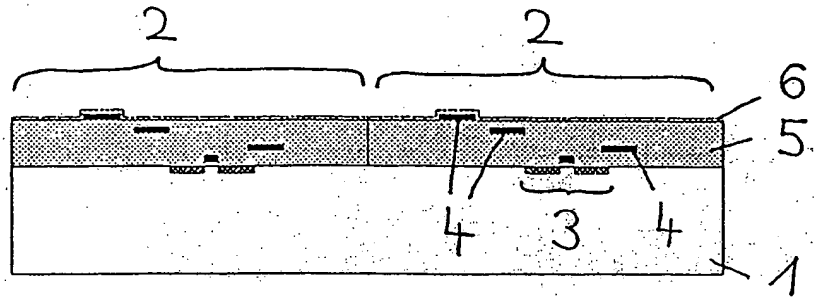

Fig. 1

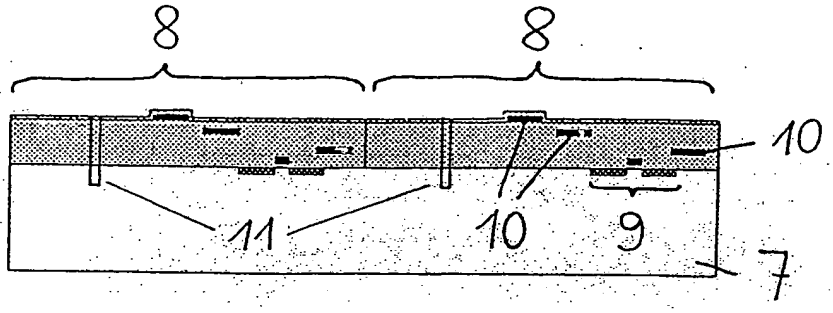

Fig. 2

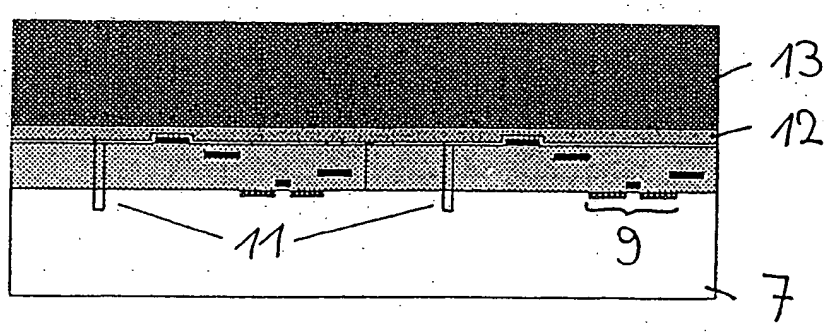

Fig. 3

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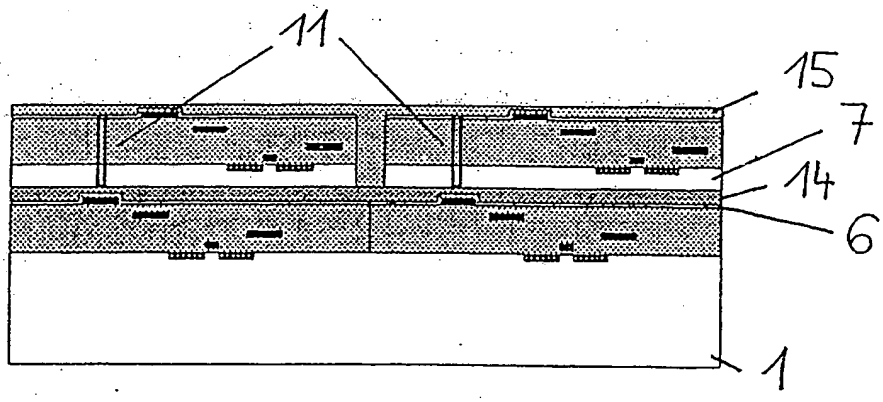

Fig. 4

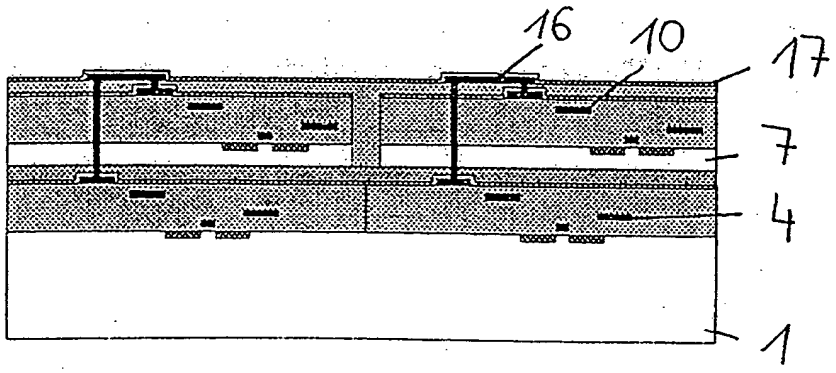

Fig. 5

Prior Art

Fig.18

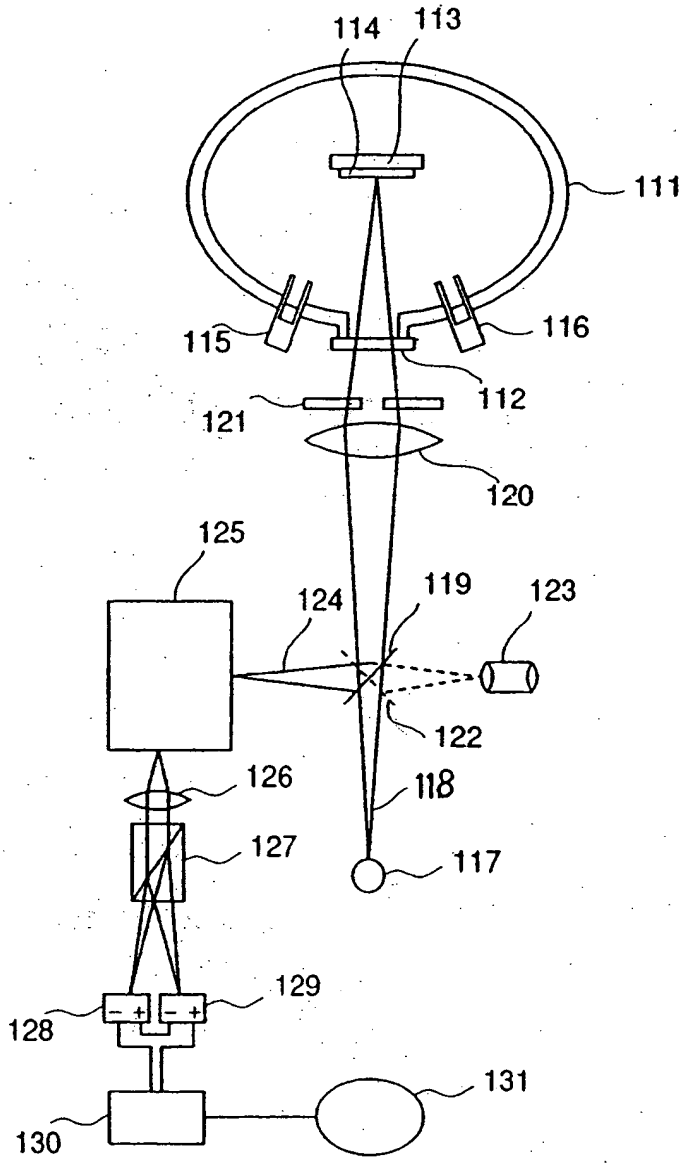

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Fig.17 (a)

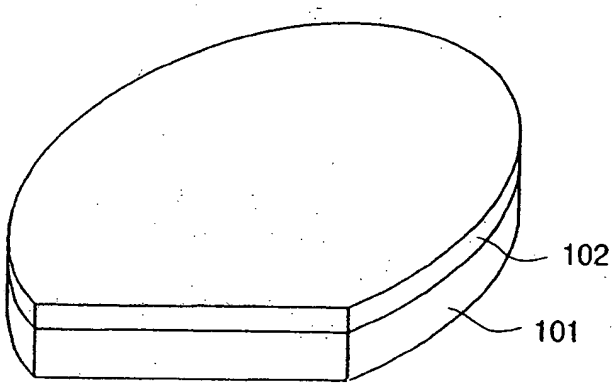
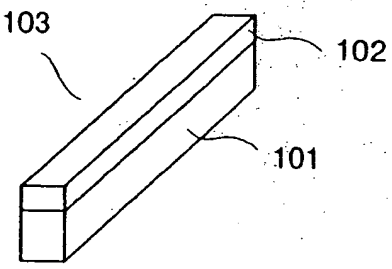
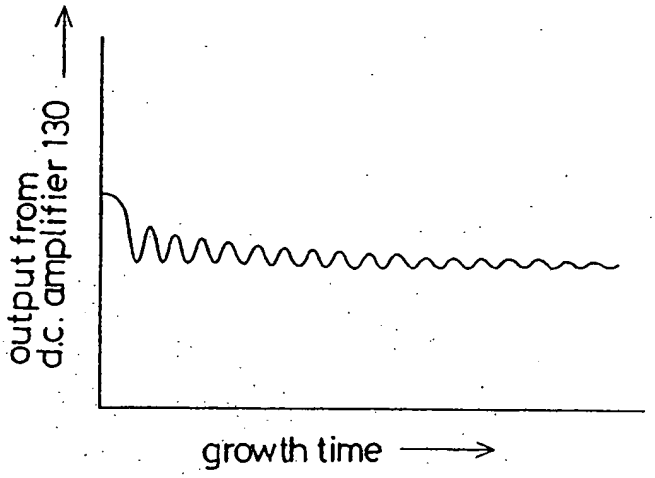


Fig.17 (b)



Prior Art

Fig.19



Prior Art

Fig.20 (a)

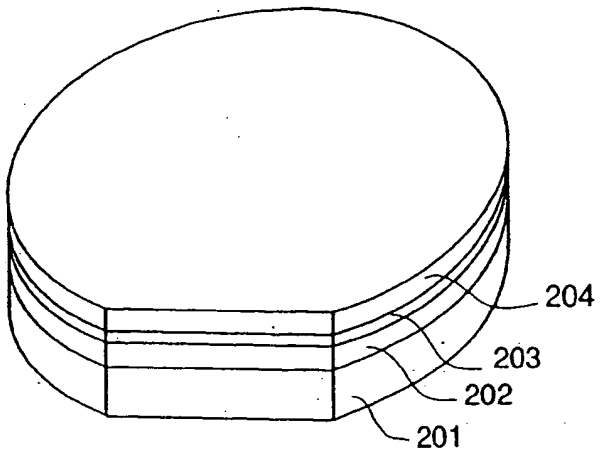


Fig.20 (b)

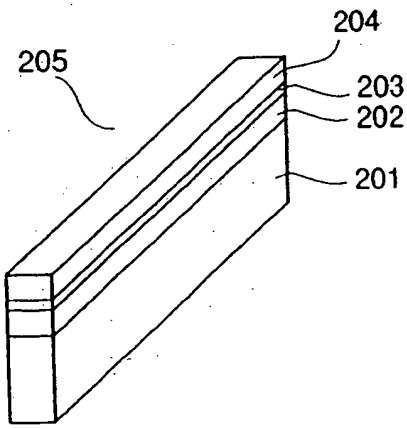


Fig. 21 (a)

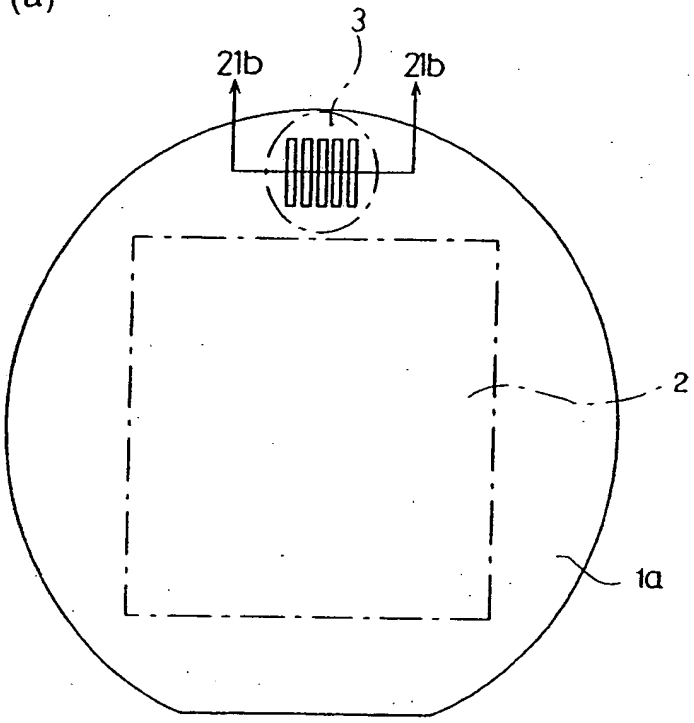
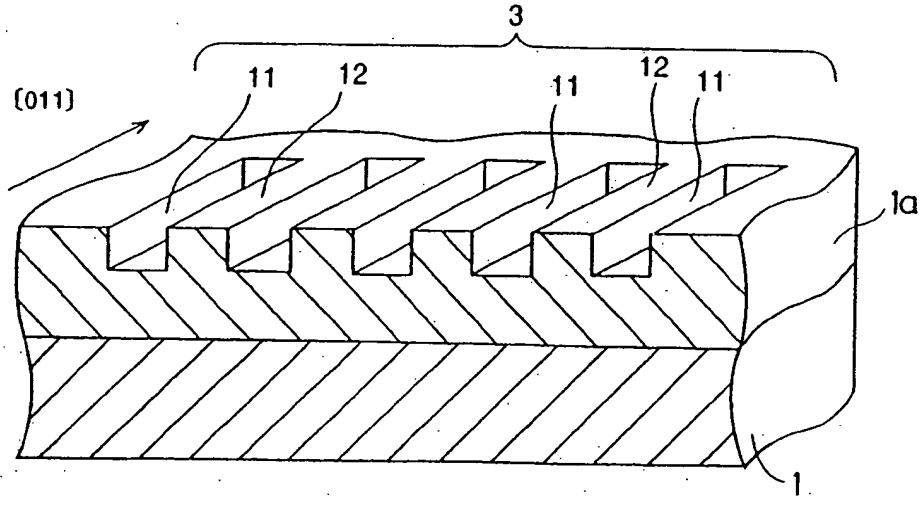


Fig. 21(b)



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(54) Method for evaluating epitaxial layers and test pattern for process evaluation.

(57) In a method for evaluating thickness of a semiconductor layer (20) epitaxially growing on a main surface of a substrate (1), a plurality of stripe-shaped ridges (12) extending in a prescribed direction are formed on the surface of the substrate, and a semiconductor layer (20) is epitaxially grown on the surface of the substrate including the stripe-shaped ridges while irradiating the stripe-shaped ridges with light (21) and monitoring diffracted light (22,23) from the stripe-shaped ridges to evaluate the thickness of the epitaxially growing semiconductor layer. Therefore, the thickness of the epitaxial layer is evaluated with high precision during the epitaxial growth process.

Fig.3 (a)

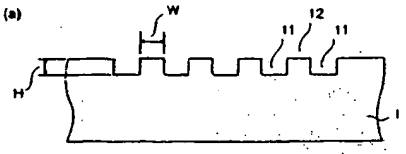


Fig.3 (b)

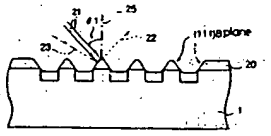
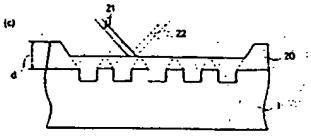


Fig.3 (c)



EP 0 632 494 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 10 8625

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
A	PATENT ABSTRACTS OF JAPAN vol. 15, no. 179 (E-1064) 8 May 1991 & JP-A-03 041 720 (NTT) * abstract *	1-9	H01L21/66
A	PATENT ABSTRACTS OF JAPAN vol. 11, no. 217 (E-523) 14 July 1987 & JP-A-62 035 635 (NTT) * abstract *	1-9	
A	EP-A-0 061 237 (ATLANTIC RICHFIELD)		
A	EP-A-0 490 186 (SHIN-ETSU HANDOTAI)		

TECHNICAL FIELDS SEARCHED (Int.Cl.5)

H01L

~~The present search report has been drawn up for all claims~~

Place of search	Date of completion of the search	Examiner
THE HAGUE	14 June 1995	PROHASKA, G

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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D : document cited in the application
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EP 94108625.8

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claims:

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

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☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☒ None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims: 1-9

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

Claims 1-9 : Measurement of thickness of epitaxial layer by the measurement of diffraction on a grating.

Claims 10 : Measurement of thickness and composition of an epitaxial AlGaAs layer on a variable width test structure by photoluminiscence.